Technical Manual CC133
12 Channel Incremental Encoder Interface With Isolated Inputs
Version 1.2 February 1991

Chapter 1

General Information

1.1 Introduction

This manual provides general information, instructions for preparation for use, installation instructions and theory of operation for the CC133 Incremental Encoder Interface for the VMEbus.

The VMEbus board can determine the rotation or translation, direction and displacement of up to twelve mechanical devices or axis, based on two input signals from transducers in quadrature.

1.2 Features

The features of the CC133 module include:

VMEbus

- VMEbus slave interface (A16;D16)
- Flexible base address selection
- Interrupter I(1-7)DYN
- Selectable Address Modifier decoding
- Occupies 256 memory locations

Channel Grouping

- 4 independent groups of 3 channels
- each group has:
- a D25 front panel connector
- an interrupt level
- an interrupt vector
- a mode register
- a device reset register
- a DC/DC converter
- two CF32006 devices in a master/slave configuration
- each group is galvanically isolated from each other and from the system

Channel Configuration

- 2 quadrature inputs
- 1 index input
- 1 digital input
- 32 bit up/down counter

- direct digital input register
- change of state detection circuit
- interrupt mask register
- enable index register
- index status register

Input Signal Configuration

- Differential, or
- Single Ended

1.3 General Description

The CC133 Twelve Channel Incremental Encoder Interface module is a VMEbus slave module. The module decodes the address lines A1 to A15 and responds when receiving the address modifier codes $29 and/or $2D (short supervisory/non-privileged I/O access). The module appears to the system as 256 byte locations which can be placed on any 256 byte boundary in the 64 kbyte short I/O space.

The module consists of 12 input channels with four differential inputs each. The channels are grouped in four independent groups. Each group is based upon two CF32006 triple incremental encoder counters and has its own synchronization and control logic.

The power of the differential receivers of each group is supplied by a separate DC/DC converter and the outputs of the receivers are optically isolated from the inputs of the synchronization circuitry. An isolation of 500 V is maintained between the input groups and between a group and the system.

Each input channel has two Quadrature input signals, one Index input and one Digital input. The Index input may reset the corresponding counter and/or generate an interrupt. The polarity of the Index input is programmable.

The Index and the Digital input create a two bit digital input channel. Each group has 6 digital inputs. A change of a digital input line of a group can be detected and may generate an interrupt when a change is detected. The interrupter is a MC68153 Bus Interrupter Module (BIM) which has a software programmable interrupt level, interrupt vector and interrupt mask register for each of the four channel groups.

1.4 Ordering Information

The following versions of the CC133 are available:

Table 1-1 Ordering Information

Module	Number of Channels
CC133-3	3
CC133-6	6
CC133-9	9
CC133-12	12

1.5 Related Documents

The following manuals are also relevant:

Table 1-2 List of Documents

Document Title	Published By
The VMEbus Specification Manual (ANSI/IEEE 1014-1987, IEC 821 and 927	VITA
CF32006 Triple Incremental Encoder Interface Data sheet	Texas Instruments

Chapter 2

Specifications

2.1 Introduction

This chapter provides a summary of the components, and a detailed specification of the module. The CC133 is a highly-integrated and high-performance VMEbus incremental encoder interface module based on the CF32006 Triple Incremental Encoder Interface.

2.2 Components Used

The CF32006 Triple Incremental Encoder Interface Chip consists of three identical incremental encoder interface circuits. This encoder interface can be configured into one of three operating modes: direction discrimination with five modes of counter incrementation, pulse width measurement, and frequency measurement.

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microprocessor system. An interrupt request from any device is routed to the MC68153, and the BIM handles all interfacing to the VMEbus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

2.3 VMEbus Options

Data Transfer Options

- DTB Slave A16;D16,D8: RMW,ADO
- Selectable AM codes: $29,$2D

Interrupter Options

- I(1,2,3,4,5,6,7)DYNAMIC INTERRUPTER
- Release on Acknowledge(ROAK)
- Release on Register Access(RORA)
- D08(O) Status/ID byte

Power Options

- 2,5A TYP (3.1A MAX) at +5 VDC

Physical Configuration Options

- Double-Height Eurocard format
- Single-Width front panel

Environmental Requirements

- Operating Temperature: 0-70 degrees C
- Max. operating humidity: 90%

2.4 Input Specifications

Input Signals

- Differential Mode Receivers conform to RS-422-A
- Single ended TTL level input signals are posible when additional resistors are placed.

Input Frequency

- Maximum Frequency of all input signals:1 Mhz

Isolation

- Channel Group to System: 500 Volt
- Channel Group to Channel Group: 500 Volt

Chapter 3

Functional Description

3.1 Introduction

This chapter provides an overview of the CC133 module, and a detailed description of each functional section. The block diagram of the module is shown in Appendix A.

3.2 Group Description

The twelve available input channels on the CC133 are divided into four identical, independent groups: Group A - Group D. Each Group is built up around two cascaded CF32006 triple incremental encoder interface circuits. The next paragraphs will describe the functions of a single Group.

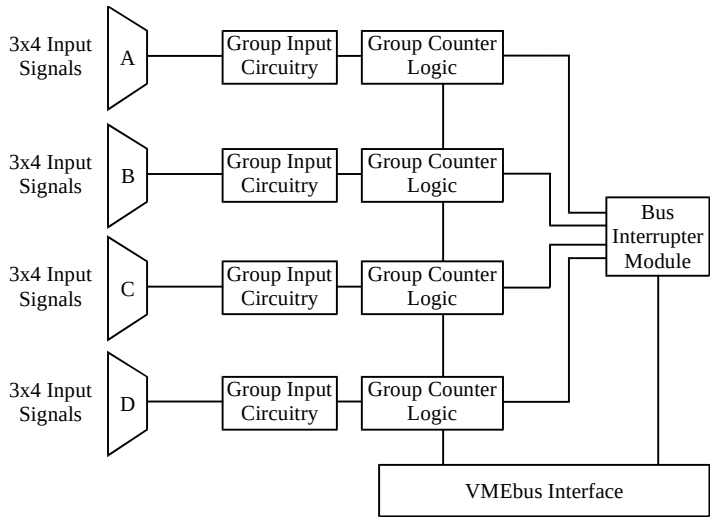

Figure 3-1 Input Groups

3.2.1 Group Input Circuit

Figure 3-2 shows a function diagram of the input circuit for each Group on the CC133.

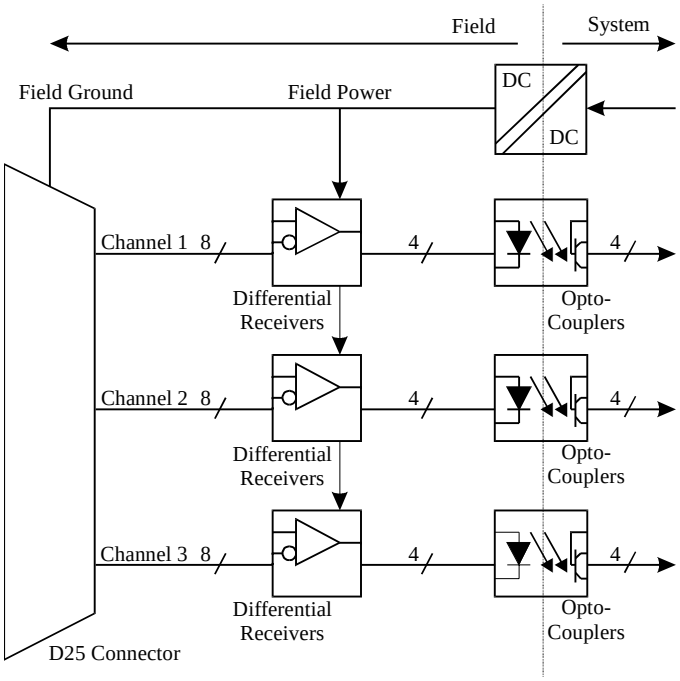

Figure 3-2 Group Input Circuit

The input signals are passed via a D25 male connector to the CC133. Each D25 connector receives the signals for three channels. The differential input signals are converted to standard TTL signals using differential receivers. The differential receivers meet the requirements of the RS-422-A standard. Each group of differential receivers is powered by a separate DC/DC converter.

The 'minus' inputs can be set to 1.6Volt, to let the 'plus' inputs accept TTL level single ended input signals.

Opto-couplers are used for galvanic isolation between the differential receivers and the system.

3.2.2 Channel Description

Each channel of the CC133 consists of four signals: two Quadrature signals, one Index signal and one Digital Input signal.

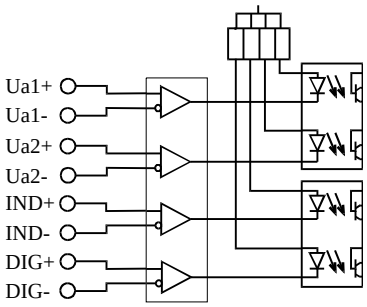

Figure 3-3 Channel Input Circuit

The Quadrature signals are used to supply information from the field to the control system. The information is translated by the encoder circuits into numeric values. The logic levels of the Quadrature signals and their relative edges will result in an increment or decrement function of the encoder counters, depending on the current operating mode of the encoder circuits.

The Index signal can be used to reset the encoder counters and generate an interrupt to the VMEbus. The Digital Input signal can serve several functions within the working environment, and can also be used to generate an interrupt to the VMEbus. The interrupt capability of both signals is fully described in the next section.

3.2.3 Interrupt Capability

Each Group on the CC133 can generate an interrupt request, independent of the other groups. As described earlier in this section each channel has two possible interrupt sources: the Digital Inputs signal and the Index signal. A Group therefore has six interrupt sources. When any of the six input signals changes its level, an interrupt can be generated.

A special 'Compare State Circuit' is implemented on the CC133 to accomplish this function. The next figure shows how this circuit is functionally implemented.

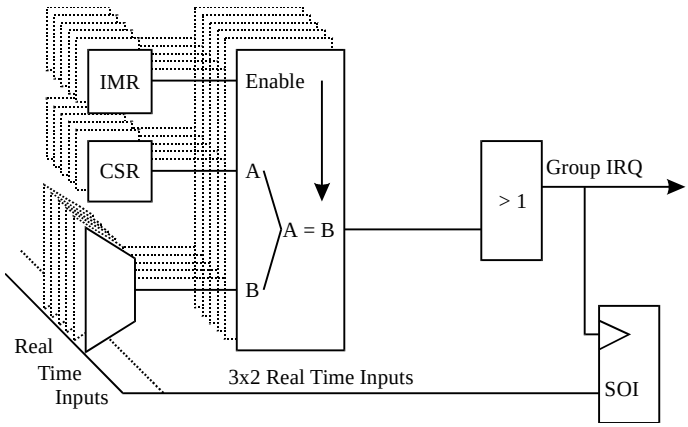

Figure 3-4 Compare State Circuit

Several registers are implemented on the CC133 for generating and controlling of the interrupt capability. Each channel has the following interrupt control/status registers:

- Direct Input Register
- Compare State Register (CSR)
- State on IRQ Register (SOI)
- IRQ Mask Register (IMR)

To detect a change in the input lines, the comparator must compare the 'Real Time' input lines with a copy of the previous state of the input lines. A copy is made of the current state of the input lines by reading the 'Direct Input Register', and this data should be written into the 'Compare State Register'. An interrupt will be generated as soon as the 'Real Time' input changes and the corresponding input is enabled in the 'IRQ Mask Register'. The current states of the Index and Digital Input signals are saved in the State On IRQ register at the time of the interrupt request. Each group has its own interrupt request signal to the Bus Interrupter Module.

Further detailed programming considerations are given in chapter 5.

3.2.4 Group Operation Modes

The CF32006 encoder circuit can work in eight different modes. The mode of operation is programmed into the encoder circuit by writing the mode number to the Mode Register of the specific Group.

Note: Different modes cannot be used inside one Group.

3.2.5 Mode Description

There are eight different modes of operation on a CF32006 encoder circuit: one counter mode, five direction discriminator modes, one mode to measure a pulse width, and one mode to measure the frequency of a signal.

3.2.5.1 Counter Mode, 0

Using the cascaded configuration (32 bit counter), the Most Significant Counter (MSC) must operate in the counter mode. With this mode, the MSC reacts only on the up and/or down pulse from the Least Significant Counter (LSC). The MSC device is hardwired to this mode.

Note: The LSC should not be asserted in the counter mode, since this will not result in any reaction when Quadrature signal levels are changed.

3.2.5.2 Direction Discriminator Modes, 1-5

A channel's Quadrature signals Ua1 and Ua2, identify forward or backward directions. If Ua1 leads Ua2, the forward direction is indicated and the counter will count up; if Ua1 lags Ua2, the reverse direction is indicated and the counter will count down.

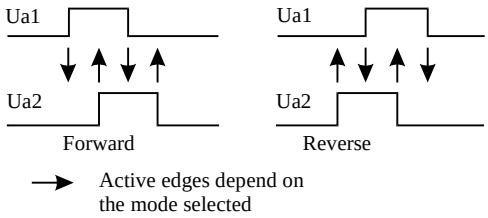

Figure 3-5 Direction Discriminator Modes

The next figure (figure 3-6) shows the five available direction discriminator modes, and the reaction of the encoder circuit to these modes. This figure shows the waveforms which force the encoder circuit to generate pulses for counting up.

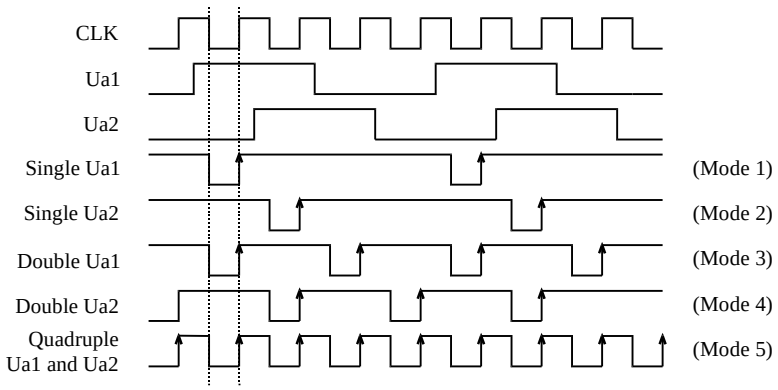

Figure 3-6 Direction Discriminator Up Clock

Figure 3-7 shows the waveforms which must be used for down counting, and gives all five direction discriminator modes.

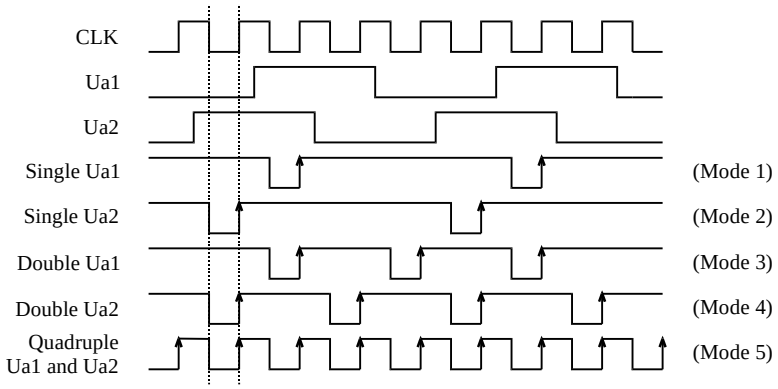

Figure 3-7 Direction Discriminator Down Clock

3.2.5.3 Pulse Width Measurement Mode, 6

In this mode Ua1 gates the pulse width to be measured. When synchronized with the clock edge after a low to high transition in Ua1, counting begins at the input clock frequency (10 MHz). Similarly, when synchronized with the clock edge after a high to low transition of Ua1, counting is disabled; the value in the counter is stored in the Channel Counter Output Register and the counter is cleared. If Ua2 is held high the counter will count up, and if Ua2 is held low the counter will count down.

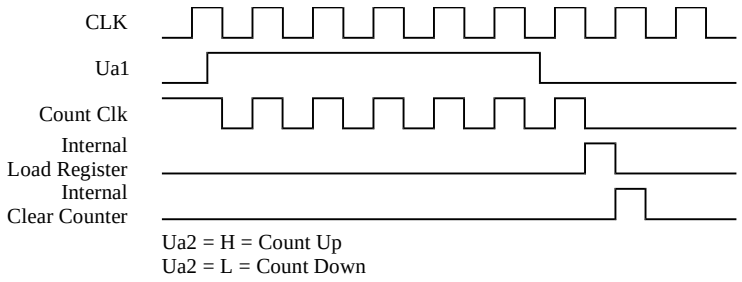

Figure 3-8 Pulse Width Measurement

3.2.5.4 Frequency Measurement Mode, 7

In Mode 7, Ua1 carries the signal of unknown frequency to be measured, and Ua2 is a gate signal of known width. A low to high transition of the Ua2 signal enables counting at the frequency of Ua1. When the gate Ua2 goes low, counting is disabled, the value is stored again in the Channel Counter Output Register, and the counter is cleared.

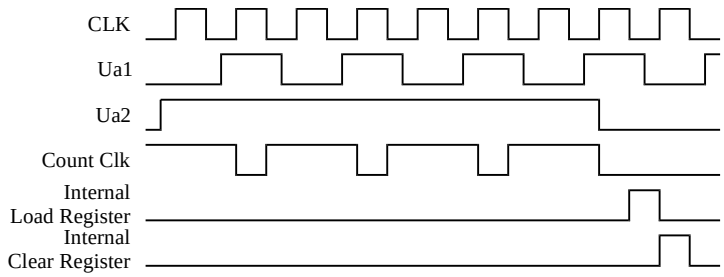

Figure 3-9 Frequency Measurement

3.2.6 Reset Operation

A total Reset is initiated by a write access to the group reset register. Depending on the state of the quadrature signals, the counters can be cleared, or set to +/- 1. To avoid this count error (+/- 1) after the

reset, the Ua1n and the Ua2n inputs should be held to the values indicated in table 3-1 during and just after the write access. It is recommended to check if the counters are cleared after the group reset.

Table 3-1 Reset Operation

Mode	Ua1n	Ua2n
0	X	X
1-5	H	H
6-7	L	L

3.3 Bus Interrupt Module

The Bus Interrupter Module on the CC133 generates interrupt requests to the VMEbus and handles Interrupt acknowledge cycles.

For each Group on the CC133, the Interrupt capability is enabled/disabled by writing to the corresponding control registers of the BIM. In addition, each Group has its own interrupt vector, which is used during the interrupt acknowledge cycle.

Chapter 4

Installation Procedures

4.1 Introduction

This chapter provides hardware preparation and installation instructions for the CC133 Incremental Encoder Module.

4.2 Installation

The module is shipped in an anti-static container which protects it against static electricity. When the module is unpacked, avoid touching areas of integrated circuitry to prevent static discharge from damaging the circuits.

The module can be used in VMEbus compatible systems and can be configured to suit many applications.

The pin definition of the VMEbus P1, P2 and the I/O connectors P3,P4,P5 and P6 can be found in Appendix B.

NOTE: ENSURE THAT THE POWER IS TURNED OFF BEFORE INSERTING OR EXTRACTING THE CC133 MODULE IN OR FROM THE SYSTEM BACKPLANE.

4.3 Address Selection

The CC133 module occupies 256 memory locations in the Short I/O space. The base address can be installed on any 256 byte boundary using hex switches SW1 and SW2. SW1 is used to set the Most significant nibble of the base address (A15-A12). SW2 is used to set the Least significant nibble of the base address (A11-A8).

4.4 Jumper Settings

The jumper setting discussed in the following section is illustrated as seen from the component side with both VMEbus connectors downwards.

4.4.1 Jumper JB1 - Access Mode

When the connection is made between pins 1 and 2 of JB1, the module will respond to both Supervisory AM code $2D and non privileged AM code $29. When pins 2 and 3 are connected, the module will respond only to the Supervisory AM code $2D.

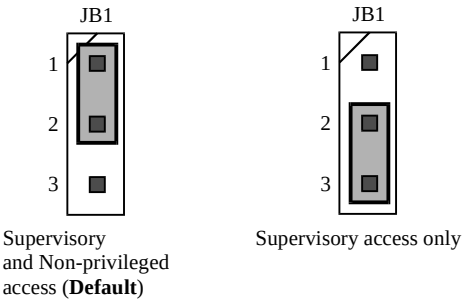

Figure 4-1 Jumper JB1 - Access Mode

4.5 Input/Output Connections

The inputs for each channel are made available at the front panel P3,P4,P5 and P6 D-25 male connectors. The next table shows the connector assignments for each channel.

Table 4-1 Channel Connector Assignments

Connector	Group	Channels
P3	A	1-3
P4	B	4-6
P5	C	7-9
P6	D	10-12

Appendix B shows the connector pin assignments for the CC133 module.

4.6 Differential Inputs

Two resistor network sockets are positioned parallel to the group's input connector. When differential input signals are required for a group, be sure the input resistor networks are removed.

4.7 Single Ended Inputs

Two resistor network sockets are positioned parallel to the group's input connector. When single ended TTL input signals are required for a group, the input resistor networks (4608X-104-302/622) have to be inserted in the sockets.

Note: Connect the TTL input signal to the 'plus' input and leave the 'minus' input open.

Table 4-2 Single Ended Mode Resistors

Channel		
Group	**Numbers**	**Resistor Networks**
A	1-3	RN34 and RN35
B	4-6	RN36 and RN37
C	7-9	RN38 and RN39
D	10-12	RN40 and RN41

Chapter 5

Operating Instructions

5.1 Introduction

This chapter provides the operating instructions for the CC133 module and also all necessary information for system programmers to take full advantage of the features of the module. The descriptions will include implementation dependent programming information that can not be found in data sheets.

The memory map of the CC133 is divided into four identical sections. Each part, or group, contains the registers of three channels.

Table 5-1 Global Memory Map

$00	Group A Registers Channels 1, 2 & 3
$40	Group B Registers Channels 4, 5 & 6
$80	Group C Registers Channels 7, 8 & 9
$C0	Group D Registers Channels 10, 11 & 12

5.2 Device Group Registers

Each device group consists of three sets of channel registers, a mode register, a reset register and two BIM (Bus Interrupter Module) registers.

Each group has its own set (master/slave) of two TCHT12316 devices.

Table 5-2 Device Group Registers

$00	Channel 1 Registers
$10	Channel 2 Registers
$20	Channel 3 Registers
$33	Group Mode Register
$37	Group Reset Register
$3B	Group BIM Control Reg
$3F	Group BIM Vector Reg

5.2.1 Channel Registers

A channel consists of a set of registers described in the following paragraphs. The address of the registers can be calculated by adding the 'group offset' and the 'channel offset' to the board base address.

Table 5-3 Channel Registers

$00	MSW Counter
$02	LSW Counter
$05	Enable Index Register
$07	Index Status Register
$09	Direct Input Register
$0B	Compare Status Register
$0D	State On IRQ Register
$0F	IRQ Mask Register

5.2.1.1 Counter

When one byte is read, the encoder chip generates a load output latch pulse for the four bytes of the Counter register. From that time until the next system reset, the load output latch pulse will only be generated during a read operation if this same byte is read. Special care should be taken if reading individual bytes to ensure that these operations are always performed in the same order.

Channel Offset	7	6	5	4	3	2	1	0	Read/Write
$00	C31	C30	C29	C28	C27	C26	C25	C24	
$01	C23	C22	C21	C20	C19	C18	C17	C16	
$02	C15	C14	C13	C12	C11	C10	C9	C8	
$03	C7	C6	C5	C4	C3	C2	C1	C0	

Figure 5-1 Channel Counter Registers

5.2.1.2 Enable Index Register

Channel Offset	7	6	5	4	3	2	1	0	Read/Write
$05							LVIND	END	

Figure 5-2 Enable Index Register

EIND When EIND=1, an index pulse will reset the counter.
When EIND=0, the index pulse is masked and will not reset the counter.

LVLIND When LVLIND=0, a '1-0-1' pulse on the index input will clear the counter, if enabled using EIND.

When LVLIND=1, a ’0-1-0’ pulse on the index input will clear the counter, if enabled using EIND.

After a SYSRESET these bits are cleared.

Note: The state of the EIND bit does not affect the interrupt capability of the index input.

5.2.1.3 Index Status Register

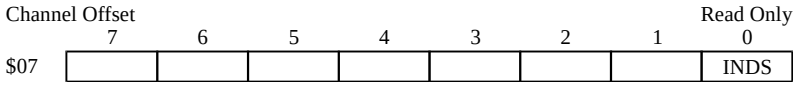

Figure 5-3 Index Status Register

INDS When INDS=1, an index pulse has occurred. This bit is cleared after the Index Status Register has been read; it can only be set when the EIND bit in the ’Enable Index Register’ is set.

5.2.1.4 Direct Input Register

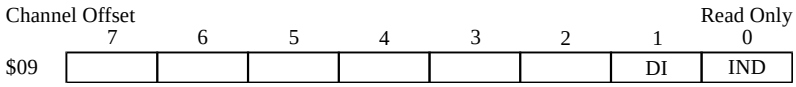

Figure 5-4 Direct Input Register

DI,IND these bits directly reflect the state of the channel’s digital input signal (DI) and the channel’s Index input signal (IND).

5.2.1.5 Compare State Register

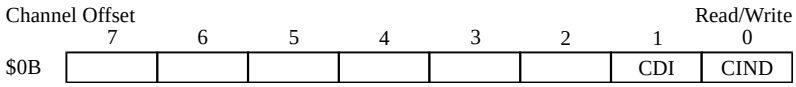

Figure 5-5 Compare State Register

When the digital inputs differ from the values of CDI and CIND written in this register, an interrupt can be generated and a sample of the digital inputs is made in the ’State On IRQ Register’

After an interrupt is generated due to a change of state, a write access to the Compare State Register should be performed before another interrupt will be detected in the specific group. The write access to the Compare State Register will clear the interrupt request to the BIM. If the IRE bit in the Group BIM Control Register is set before the Compare State Register is written, another interrupt will be generated.

5.2.1.6 State On IRQ Register

Channel Offset	7	6	5	4	3	2	1	0
								Read Only
$0D							SDI	SIND

Figure 5-6 State On IRQ Register

The SDI and SIND bits reflect the state of the digital inputs the moment they differ from the 'Compare State Register' and an interrupt request is made to the Bus Interrupter Module.

5.2.1.7 IRQ Mask Register

Channel Offset	7	6	5	4	3	2	1	0
								Read/Write
$0F							MDI	MIND

Figure 5-7 IRQ Mask Register

MDI When this bit is set, a difference between the DI bit and the CDI bit will cause an interrupt request to the Bus Interrupter Module (BIM).
When MDI=0, a change of state of the channel's DI bit will not generate an interrupt to the BIM.

MIND When this bit is set, a difference between the IND bit and the CIND bit will cause an interrupt request to the Bus Interrupter Module (BIM).
When MIND=0, a change of state of the channel's IND bit will not generate an interrupt to the BIM.

After a SYSRESET these bits are cleared.

5.2.2 Group Mode Register

Group Offset	7	6	5	4	3	2	1	0
								Read/Write
$33						M2	M1	M0

Figure 5-8 Group Mode Register

The 'Group Mode Register' is used to set the mode of the group's CF32006 master device. The slave device is always in mode 0.

The following modes can be selected for the master device.

Table 5-4 CF32006 Modes

Mode	M2	M1	M0	Description
Counter				
0	0	0	0	16-bit up/down counter (inhibits direction discriminator)
Direction Discriminator				
1	0	0	1	Single count pulse synchroneous with Ua1 rising in forward direction and Ua1 falling in backward direction.
2	0	1	0	Single count pulse synchroneous with Ua2 rising in forward direction and Ua2 falling in backward direction.
3	0	1	1	Double count pulse synchroneous with Ua1 rising and falling.
4	1	0	0	Double count pulse synchroneous with Ua2 rising and falling.
5	1	0	1	Quadruple count pulse synchroneous with all edges.
Pulse Width Measurement				
6	1	1	0	Ua1 is the gate signal. Ua2 is high for up counting and low for down counting. Count is synchroneous with rising clock.
Frequency Measurement				
7	1	1	1	Ua1 is frequency signal to be measured. Ua2 is the gate signal of known time interval. Count is synchroneous with rising edge of Ua1

5.2.3 Group Reset Register

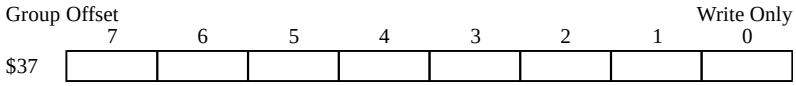

Figure 5-9 Group Reset Register

A write access to the 'Group Reset Register' will generate a master reset signal to the group's CF32006 device. The mode control logic is reset to a known state, and the counters are cleared.

5.2.4 Group BIM Control Register

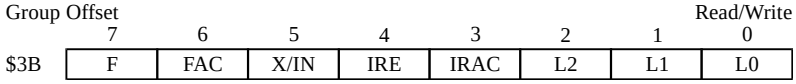

Figure 5-10 Group BIM Control Register

L2,L1,L0 Interrupt level. These bits determine the level at which an interrupt will be generated. A value of zero disables the interrupt.

IRAC Interrupt Auto Clear. If the IRAC bit is set(bit 3), IRE (bit 4) is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the 'Group BIM Control Register'

IRE Interrupt Enable. This bit must be set to enable the bus interrupt request associated with this register. Thus, if the INTx input line is asserted and IRE is cleared, *no* interrupt request will be asserted.

X/IN External/Internal.
When this bit is cleared, the IRQ Vector from the 'Group BIM Vector Register' is presented on the data lines during an interrupt acknowledge cycle.
When this bit is '1' BIM does not supply the vector.

Note: This bit must always be programmed to 0 because there is no other on-board vector source.

FAC Flag Auto Clear. If the FAC bit is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

F Flag. Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC680xx. It can be changed without affecting BIM operation.

5.2.5 Group BIM Vector Register

Group Offset	7	6	5	4	3	2	1	Read/Write 0
$3F	V7	V6	V5	V4	V3	V2	V1	V0

Figure 5-11 Group BIM Vector Register

This byte is presented on the databus during an interrupt acknowledge cycle. After SYSRESET this register is set to $0F, the MC680xx uninitialized vector.

Appendix A Block Diagram

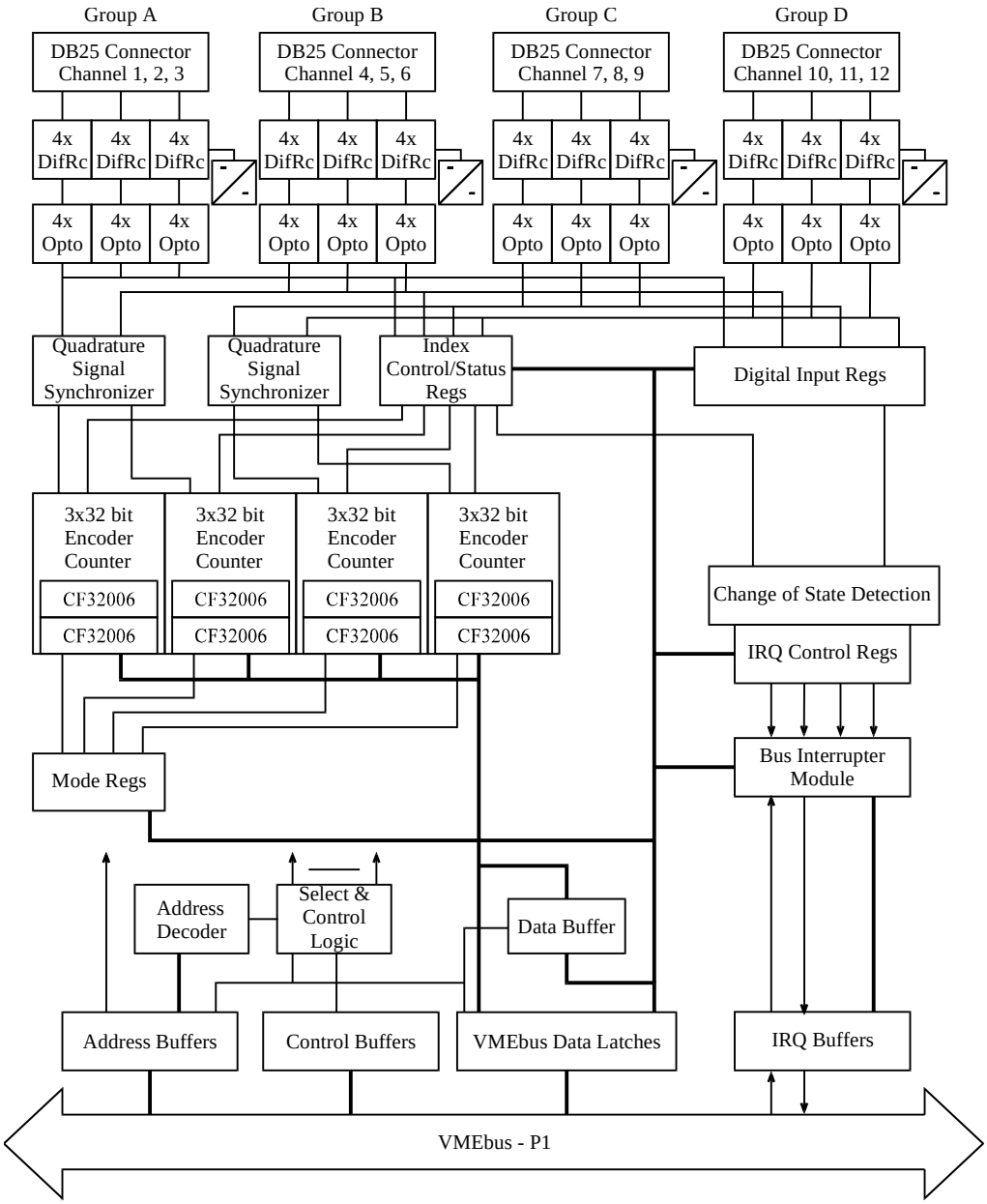

Figure A-1 Block Diagram CC133

Appendix B Connector Assignments

This Appendix identifies the VMEbus connectors P1, and P2.

Table B-1 VMEbus P1

Pin Number	(a) Signal Mnemonic	(b) Signal Mnemonic	(c) Signal Mnemonic
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12V)	(+5V STDBY)	(+12V)
32	+5V	+5V	+5V

Note: Signal mnemonics shown in parenthesis () are not used by the CC133 module.

Table B-2 VMEbus P2

P2 Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1		+5 VOLT	
2		GND	
3		(RESERVED)	
4		(A24)	
5		(A25)	
6		(A26)	
7		(A27)	
8		(A28)	
9		(A29)	
10		(A30)	
11		(A31)	
12		GND	
13		+5 VOLT	
14		(D16)	
15		(D17)	
16		(D18)	
17		(D19)	
18		(D20)	
19		(D21)	
20		(D22)	
21		(D23)	
22		GND	
23		(D24)	
24		(D25)	
25		(D26)	
26		(D27)	
27		(D28)	
28		(D29)	
29		(D30)	
30		(D31)	
31		GND	
32		+5 VOLT	

D25 Connectors P3 - P6

Four 25-pin male "D" type connectors are available on the front panel of the module. Each connector contains all signal for three input channels.

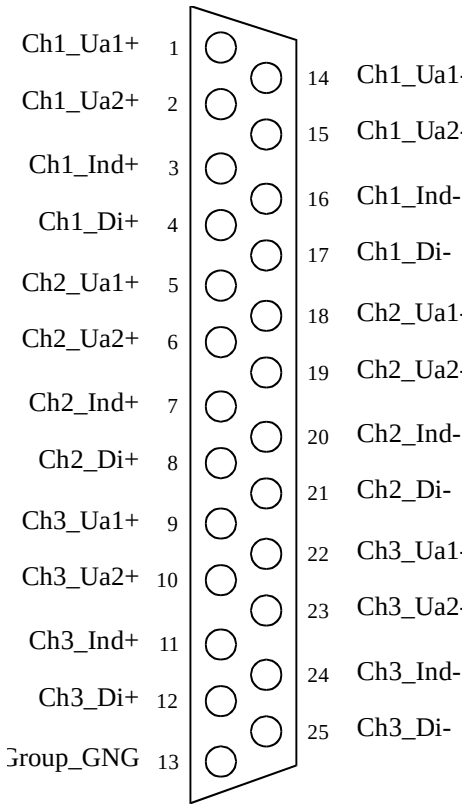

Figure B-1 D25 Connector Specification

Note: When inputs are configured to be Single Ended, connect TTL level input signals to the 'plus' inputs (pins 1-12), and leave the 'minus' inputs open (pins 14-25).

Appendix C Memory Map

Table C-1 Memory Map Group A

Name	Start	End	Size
Group A, Channel 1			
Counter	00	03	4 bytes
Enable Index Register	05	05	1 byte
Index Status Register	07	07	1 byte
Direct Input Register	09	09	1 byte
Compare State Register	0B	0B	1 byte
State on IRQ Register	0D	0D	1 byte
IRQ Mask Register	0F	0F	1 byte
Group A, Channel 2			
Counter	10	13	4 bytes
Enable Index Register	15	15	1 byte
Index Status Register	17	17	1 byte
Direct Input Register	19	19	1 byte
Compare State Register	1B	1B	1 byte
State on IRQ Register	1D	1D	1 byte
IRQ Mask Register	1F	1F	1 byte
Group A, Channel 3			
Counter	20	23	4 bytes
Enable Index Register	25	25	1 byte
Index Status Register	27	27	1 byte
Direct Input Register	29	29	1 byte
Compare State Register	2B	2B	1 byte
State on IRQ Register	2D	2D	1 byte
IRQ Mask Register	2F	2F	1 byte
Group A			
Mode Register	33	33	1 byte
Reset Register	37	37	1 byte
BIM Control Register	3B	3B	1 byte
BIM Vector Register	3F	3F	1 byte

Table C-2 Memory Map Group B

Name	Start	End	Size
Group B, Channel 4			
Counter	40	43	4 bytes
Enable Index Register	45	45	1 byte
Index Status Register	47	47	1 byte
Direct Input Register	49	49	1 byte
Compare State Register	4B	4B	1 byte
State on IRQ Register	4D	4D	1 byte
IRQ Mask Register	4F	4F	1 byte
Group B, Channel 5			
Counter	50	53	4 bytes
Enable Index Register	55	55	1 byte
Index Status Register	57	57	1 byte
Direct Input Register	59	59	1 byte
Compare State Register	5B	5B	1 byte
State on IRQ Register	5D	5D	1 byte
IRQ Mask Register	5F	5F	1 byte
Group B, Channel 6			
Counter	60	63	4 bytes
Enable Index Register	65	65	1 byte
Index Status Register	67	67	1 byte
Direct Input Register	69	69	1 byte
Compare State Register	6B	6B	1 byte
State on IRQ Register	6D	6D	1 byte
IRQ Mask Register	6F	6F	1 byte
Group B			
Mode Register	73	73	1 byte
Reset Register	77	77	1 byte
BIM Control Register	7B	7B	1 byte
BIM Vector Register	7F	7F	1 byte

Table C-3 Memory Map Group C

Name	Start	End	Size
Group C, Channel 7			
Counter	80	83	4 bytes
Enable Index Register	85	85	1 byte
Index Status Register	87	87	1 byte
Direct Input Register	89	89	1 byte
Compare State Register	8B	8B	1 byte
State on IRQ Register	8D	8D	1 byte
IRQ Mask Register	8F	4F	1 byte
Group C, Channel 8			
Counter	90	93	4 bytes
Enable Index Register	95	95	1 byte
Index Status Register	97	97	1 byte
Direct Input Register	99	99	1 byte
Compare State Register	9B	9B	1 byte
State on IRQ Register	9D	9D	1 byte
IRQ Mask Register	9F	9F	1 byte
Group C, Channel 9			
Counter	A0	A3	4 bytes
Enable Index Register	A5	A5	1 byte
Index Status Register	A7	A7	1 byte
Direct Input Register	A9	A9	1 byte
Compare State Register	AB	AB	1 byte
State on IRQ Register	AD	AD	1 byte
IRQ Mask Register	AF	AF	1 byte
Group C			
Mode Register	B3	B3	1 byte
Reset Register	B7	B7	1 byte
BIM Control Register	BB	BB	1 byte
BIM Vector Register	BF	BF	1 byte

Table C-4 Memory Map Group D

Name	Start	End	Size
Group D, Channel 10			
Counter	80	83	4 bytes
Enable Index Register	85	85	1 byte
Index Status Register	87	87	1 byte
Direct Input Register	89	89	1 byte
Compare State Register	8B	8B	1 byte
State on IRQ Register	8D	8D	1 byte
IRQ Mask Register	8F	4F	1 byte
Group D, Channel 11			
Counter	90	93	4 bytes
Enable Index Register	95	95	1 byte
Index Status Register	97	97	1 byte
Direct Input Register	99	99	1 byte
Compare State Register	9B	9B	1 byte
State on IRQ Register	9D	9D	1 byte
IRQ Mask Register	9F	9F	1 byte
Group D, Channel 12			
Counter	A0	A3	4 bytes
Enable Index Register	A5	A5	1 byte
Index Status Register	A7	A7	1 byte
Direct Input Register	A9	A9	1 byte
Compare State Register	AB	AB	1 byte
State on IRQ Register	AD	AD	1 byte
IRQ Mask Register	AF	AF	1 byte
Group D			
Mode Register	B3	B3	1 byte
Reset Register	B7	B7	1 byte
BIM Control Register	BB	BB	1 byte
BIM Vector Register	BF	BF	1 byte

Appendix D Photo CC133 Board

Placeholder

Figure D-1 Photo CC133 Board