Technical Manual CC175
Dual Channel Intelligent CAN Interface for VMEbus
Version 2.1 August 1994

Chapter 1

General Information

1.1 Introduction

This manual provides general information, preparation for use, installation instructions and theory of operation for the CC175 dual channel Controller Area Network (CAN) interface for VMEbus.

The manual also includes basic information needed by software engineers to design and implement software for the module.

1.2 Features

The features of the CC175 module include:

CAN Compatible

- Two independent CAN interface channels
- Philips 82C200 CAN controller
- ISO/DIS 11898 high speed physical interface with optical isolation

VMEbus Compatible

- VMEbus slave interface
- 7-level interrupter

Local Processor

- 16 MHz MC68000 microprocessor

Local Memory

- 1 MByte EPROM
- 1 MByte SRAM
- 4 kByte SRAM shared with VMEbus
- 512 bytes EEPROM

I/O Ports

- 2 asynchronous serial channels

Miscellaneous Functions

- Power monitor and watchdog
- 16-bit programmable timer/counter with interrupt
- 100 µs timer interrupt
- 8-bit DIP switch input
- 6 user LEDs

1.3 General Description

The CC175 dual channel Controller Area Network (CAN) interface provides a flexible and powerful connection from the VMEbus to the CAN network. The module contains two separate CAN network interface connections, each having its own controller and accompanying physical network interface.

The CAN controllers are capable of handling all CAN functions on-chip. The optical isolated physical interface is conform the ISO/DIS 11898 standard using the 82C251 CAN transceiver. To provide additional protection the interface is optically isolated using on-board optocouplers and DC/DC converters.

The on-board MPU eases the integration of the CC175 in a VMEbus system. Dual-Ported memory in combination with mailbox interrupts supports an extensive set of software options. These include both low-level CAN functions as well as standard higher protocol software layers.

1.4 Ordering Information

Table 1-1 Ordering Information

Module Name	SRAM Capacity
CC175-P-256K	256KByte
CC175-P-1024K	1 MByte

1.5 Related Documents

The following documentation can be referred to for detailed information about related items not described in this manual.

Table 1-2 List of Documents

Document Title	Published by
The VMEbus Specification Manual (ANSI/IEEE 1014-1987, IEC 821 and 927)	VITA
MC68000 16-/32-Bit Microprocessor Data Sheet	Motorola

Table 1-2 List of Documents

Document Title	Published by
SCN68681 Dual Universal Asynchronous Receiver/Transmitter (DUART)	Signetics
82C200 Data Sheet	Philips
82C251 Data Sheet	Philips

Chapter 2

Specifications

2.1 Introduction

The CC175 is a dual channel intelligent network interface module for the Controller Area Network (CAN). The CC175-P is equipped with the 82C200 CAN Controllers from Philips.The optical isolated physical interface is based on the 82C251 CAN transceiver.

The following section gives an overview of the main parts that are used.

2.2 Components Used

The MPU is a 68000 microprocessor with 32-bit data, address and stack registers. It has a 16 MByte direct addressing range, 16-bit data path and runs at 16 MHz.

The local memory consists of two 32-pin JEDEC sockets for 1-, 2- or 4-MBit type EPROMs and two 32-pin JEDEC sockets for 1- or 4-MBit type SRAMs. This configuration gives a maximum EPROM and SRAM space of 1 MByte each.

The 68681 DUART (Dual Asynchronous Universal Receiver Transmitter) has programmable operating modes and data formats for each channel. It can operate at baudrates from 50 to 38.4k Baud. Channel A has an RS-232 interface on a front panel connector. The channel B signals are available at TTL levels via the VMEbus P2 connector.

The 82C200 from Philips is a highly integrated stand-alone protocol controller for the Controller Area Network (CAN). It contains all the necessary features required to implement a high performance communication protocol. The programmable transfer rate of the 82C200 goes up-to 1 MBaud.

The 82C251 is the interface between the CAN protocol controller and the physical bus. It is intended for high speed applications up-to 1 MBaud and is fully compatible with the ISO/DIS 11898 standard.

2.3 VMEbus Options

Data Transfer Options

- DTB Slave A24;D16,D8

Interrupter Options

- Any one of I(1),I(2),I(3),I(4),I(5),I(6),I(7) (Static)
- 8-bit Status/ID
- Release On Acknowledge (ROAK)

Power Options

- 1.5 A Maximum (1.0 A Typical) at +5 VDC

Physical Configuration Options

- Double height Eurocard format

Environmental Requirements

- Operating temperature: 0 to 70 degrees C
- Maximum operating humidity: 90%

2.4 Input/Output Options

CAN Options

- Two independent CAN channels
- Each channel has its physical link available at the front and via the VMEbus P2 connector
- ISO/DIS 11898 compatible isolated physical interface

Serial Interface Options

- Asynchronous RS-232 level channel at front connector
- Asynchronous TTL level channel via VMEbus P2 connector

Miscellaneous

- Front panel LED for MPU HALT signal
- Three user programmable front panel LEDs (green, yellow and red) for each channel

Chapter 3

Functional Description

3.1 Introduction

This chapter gives an overview of the CC175 module and a detailed description of the functional sections. The block diagram of the module is given in Appendix A.

Two types of symbols are used in the schematic diagrams. One represents hierarchical components and is referenced with a component number (CMPxxx). The detailed circuit diagram of these components are shown on a separate sheet. The other type of symbol represents the actual physical components and is referenced with a corresponding letter (i.e. U for ICs, P for connectors, R for resistors, etc.). Physical components have pin numbers assigned to their symbol pins, while hierarchical components have no pin numbers.

Signal names ending with a tilde (~) or an asterisk (*) are active low.

3.2 68000 MPU

The 68000 is the main processor on the CC175. It controls all the on-board peripheral devices including the two CAN controllers. The local processor handles the data transfers between the shared memory and the CAN controllers, thereby relieving the VMEbus host processor from handling interrupts from or transferring data to the CAN controllers. The local processor can execute low level CAN functions as well as standard higher protocol software layers.

All data transfers to or from the CC175 are done by the VMEbus host processor. The local processor is not able to access resources on the VMEbus.

3.3 MPU Supervision

The DS1232 MicroMonitor Chip monitors three vital conditions: power supply, software execution and external override.

When the power supply falls below 4.75 volts, the local processor is stopped by asserting the reset and halt inputs. On power-up, reset and halt are kept active for a minimum of 250 ms to allow the power supply and processor to stabilize.

The watchdog timer function forces reset and halt low to the processor when it is not stimulated for 600 ms. After a reset, the watchdog timer is initially stimulated by the ECLK of the processor. When the processor writes to the ‘kick watchdog’ location for the first time, the ECLK is removed from the watchdog timer and the local processor must write to the ‘kick watchdog’ location every 600 ms to prevent the watchdog timer from resetting the processor.

An external override is generated via the mailbox reset function. The reset and halt signals to the processor are asserted for a period of 250 ms after a write to the mailbox reset locations.

3.4 Local Memory

Sockets are available for standard 32-pin byte-wide memory devices, including the 128k x 8, 256k x 8 and 512k x 8 type devices.
The two JEDEC sockets for EPROM are accessible for read cycles, write cycles have no effect.
The two JEDEC sockets for SRAM are accessible for read and write cycles. The upper and lower bytes can be read and written independently.

The XC24C04 EEPROM is of the serial access type and is read and written using 3 I/O lines of the DUART. The data retention is specified to be greater than 100 years.

3.5 Serial I/O

The DUART has two serial channels, several multipurpose I/O lines, and a 16-bit counter/timer. The timebase comes from a 3.6864 MHz clock generator.

Channel A is available at a connector on the front panel and has a RS-232 interface. The RS-232 driver circuit uses the single 5 volt supply to generate the ±10 volt supply voltages.
Channel B is available via the VMEbus P2 connector at TTL level.

The multipurpose I/O lines are used for controlling several functions on the board and are discussed in paragraph 5.7

3.6 Module ID

The module ID is a hexadecimal number that ranges from $0 through $1F. The Module ID provides several specific hardware functions:

- it specifies the VMEbus base address of the shared memory
- it is used in the Status/ID byte during interrupt acknowledge cycles
- it can be read by the local processor

There are two ways to set the module ID:

- Module ID jumper block is used
- VMEbus P2 signals are used

3.7 VMEbus Interface

3.7.1 Shared Memory

A 4-kByte section of the local SRAM is shared on the VMEbus. This memory can be read from or written to by the local processor as well as by a VMEbus master. The shared memory supports read-modify-write cycles from the local processor as well as from the VMEbus master.

The base address of the shared memory on the VMEbus depends on the Module ID installed. The shared memory is accessible in the standard (A24) address space, and takes 4 kBytes in the memory map starting at $C00000 + (Module ID x $1000). The shared memory takes 4 kBytes in the A24 memory map, and modules with successive module IDs will take consecutive 4 kByte memory blocks.

The on-board shared SRAM is used for communication with VMEbus masters, and a part of the shared SRAM is assigned to a mailbox. By writing to this mailbox a VMEbus master is able to interrupt or reset the local processor.

3.7.2 Interrupter Function

The interrupter can place an interrupt on a jumper selectable IRQ level. An asserted interrupt line will be negated as soon as the VMEbus master acknowledges the interrupt by reading the Status/ID byte. This is called Release On Acknowledge (ROAK).

The least significant five bits (bit 4-0) of the Status/ID byte is the Module ID. Bit 5 and 6 are hardwired to logic ‘1’. The most significant bit (bit 7) is set by the ID7 bit in the ID7 control register. The Status/ID byte ranges from $60-$FF depending on the Module ID value installed and the value of the ID7 bit.

3.8 CAN Interfaces

Two CAN Interfaces are available on the CC175 module, channel 0 and channel 1. The channels are programmed independently of each other. Each channel has a CAN Controller in combination with an optical isolated physical interface conform the ISO/DIS 11898 standard. The physical interface can be bypassed using a mezzanine module.

3.8.1 CAN Controller

The 82C200 CAN Controller is placed on the CC175. This CAN Controller executes the high performance communication protocol, and appears to the MPU as a memory-mapped I/O device.

3.8.2 CAN Physical Interface

The on-board physical interface has optical isolation between the CAN controller and the CAN transceiver. The 82C251 is used as CAN transceiver, which is intended for high speed applications.

3.9 DIP Switch

The setting of the DIP switch can be read by the MPU and used by the on-board software for user programmable purpose. There are no hardware functions connected to the DIP switch settings.

Chapter 4

Installation Procedures

4.1 Introduction

This chapter provides the preparation and installation instructions for the CC175 dual channel intelligent CAN module.

4.2 Installation

The module is shipped in an antistatic container to protect the module against static electricity. When the module is unpacked, avoid touching areas of integrated circuitry to prevent static discharge from damaging the circuits.

The module is used in VMEbus compatible systems and allows for configuration to suit many applications. Jumpers are used to select hardware specific options. The jumper block positioning and default jumper settings are illustrated in Appendix C. The pin definitions of the VMEbus P1, P2 connectors and Front Panel connectors P3, P4, P5, J1, and J2 are found in Appendix B.

NOTE: ENSURE THAT POWER IS TURNED OFF BEFORE INSERTING OR WITHDRAWING THE CC175 MODULE IN OR FROM THE SYSTEM BACKPLANE.

4.3 Jumper Settings

All jumper settings discussed in the following sections are illustrated as seen from the component side with the VMEbus connector downwards. The next table gives a summary of the default jumper settings and their functions.

Table 4-1 Default Jumper Settings

Description	Jumper Block	Default Setting	Status	Section
“IRQ Level”	JB1	1-2,3-4,5-6 Connected	Disabled	4.3.1
“MPU Clock”	JB2	2-3 Connected	16 MHz Clock	4.3.2
“Local Bus Time Out”	JB3	Not Connected	Enabled	4.3.3
“EPROM Size”	JB4	1-2 Connected	1 or 2 MBit Devices	4.3.4
“Module ID”	JB5	Not Connected	ID is $1F	4.3.5
“System Clock”	JB6	2-3 Connected	Use Local Oscillator	4.3.6
“Speed Control”	JB7 JB8	2-3 Connected	High Speed	4.3.7

Table 4-1 Default Jumper Settings (Continued)

Description	Jumper Block	Default Setting	Status	Section
“Physical Interface Input”	JB9 JB10	3-4,5-6,7-8,11-12 Connected	Use On Board Interface	4.3.8
“Physical Interface Output”	JB11 JB12	3-4,5-6,11-12,13-14 Connected	Use On Board Interface	4.3.9
“SRAM Size”	JB13	1-2 Connected	1 MBit Devices	4.3.10

4.3.1 IRQ Level

The setting of jumper block JB1 defines which interrupt line will be asserted during an interrupt request to the VMEbus.

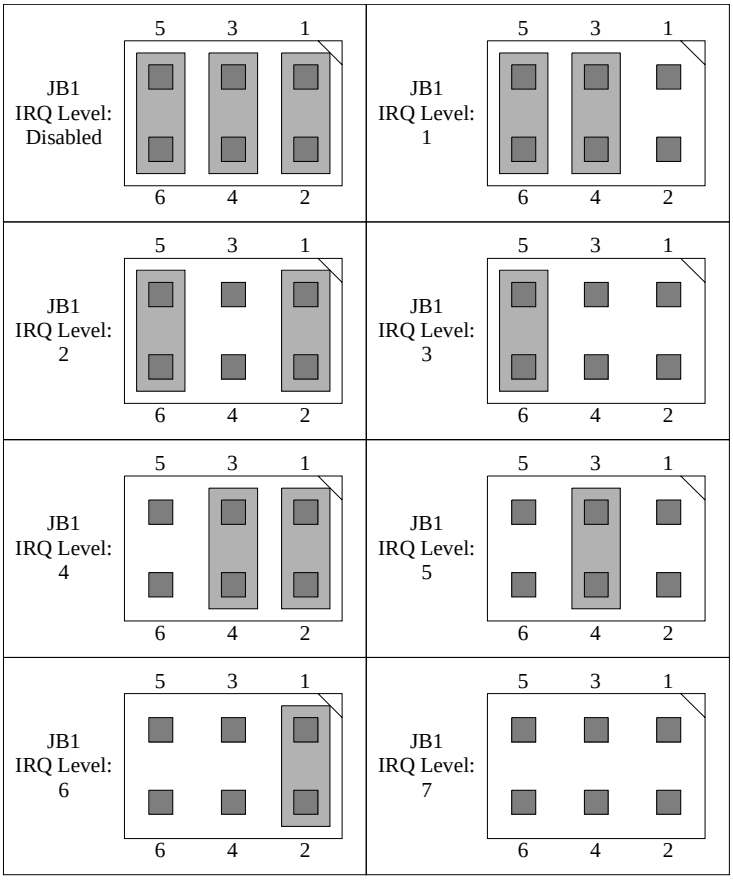

Figure 4-1 Interrupt Request Level

4.3.2 MPU Clock

Jumper JB2 is used to select the MPU clock rate.

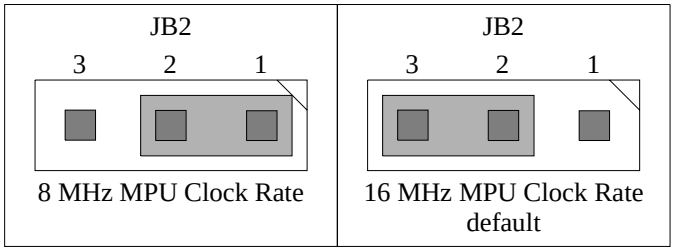

Figure 4-2 MPU Clock Select

It may be useful to let the 16 MHz processor run at 8 MHz when using a standard (slow) logic analyser or emulator during the application debugging phase.

4.3.3 Local Bus Time Out

Jumper JB3 is used to select the local bus time out function. When no jumper is installed (default), the bus time out circuit will generate a Bus Error response to the MPU, when a bus access (Address Strobe active) is not acknowledged within 2.4 µs.

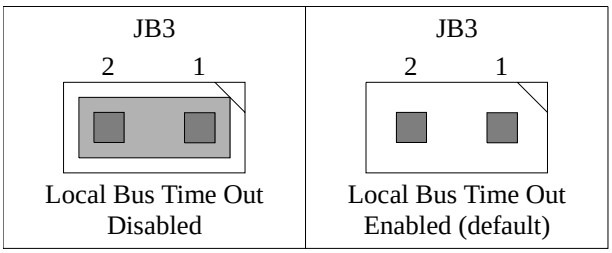

Figure 4-3 Local Bus Time Out Select

4.3.4 EPROM Size

The U7-U8 socket pair is used for EPROM devices and may contain 1, 2, or 4 MBit type EPROMs. Device U7 is read at odd addresses and U8 at even addresses

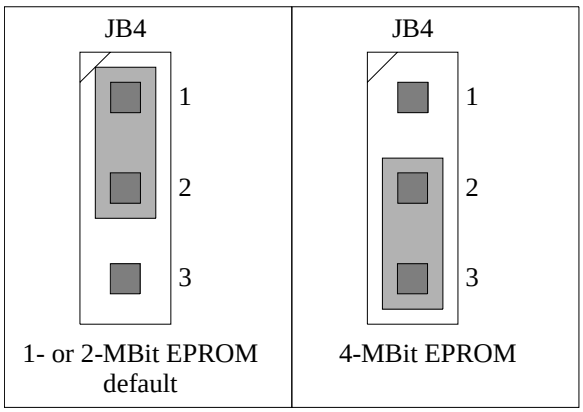

Figure 4-4 EPROM Size Select

EPROM devices must have a speed of 250 ns (or faster).

4.3.5 Module ID

The Module ID can be set in two ways: by using the VMEbus P2 connector signals or by using the JB5 Module ID jumper block.

The Module ID signal lines MID4 to MID0 are held in a high (1) level by pull-up resistors. These signal lines can be asserted to a low (0) level by either inserting jumpers on the JB5 jumper block or by connecting the MID4 to MID0 signals to ground on the VMEbus J2 backplane.

When the VMEbus P2 signal option is used then all jumpers on JB5 must be removed. The VMEbus option allows for a geographical addressing of the module. That means that the slot position of the module defines the VMEbus address of the module. This will prevent address conflicts when using multiple CC175 modules in one system. See the VMEbus P2 connector assignments for the MID4 to MID0 signal pins.

When the JB5 jumper block is used then insert jumpers on the MID4 to MID0 signals to assert them to a low (0) level. In this case the VMEbus P2 signals must be left unconnected.

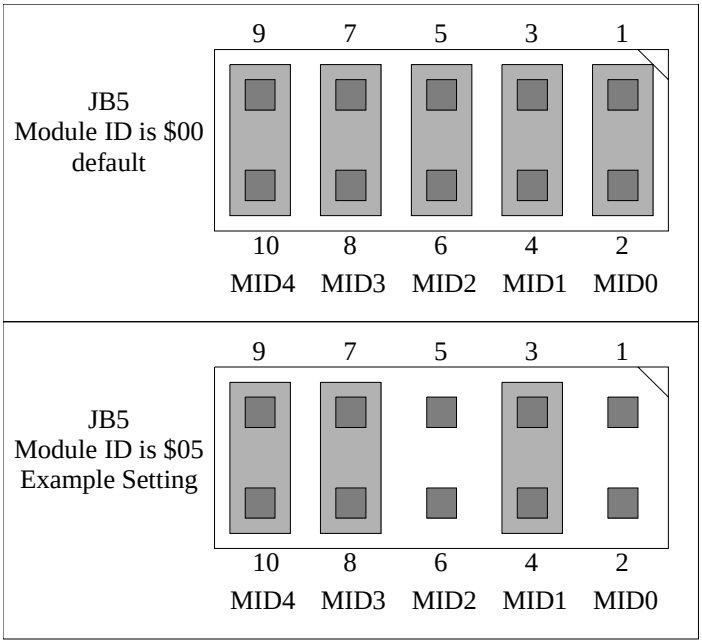

Figure 4-5 Module ID Select

4.3.6 System Clock

Jumper JB6 is used to select the source of the local system clock. The source can be the output of a local X-tal controlled oscillator or the VMEbus system clock. The local oscillator has a frequency of 16 MHz.

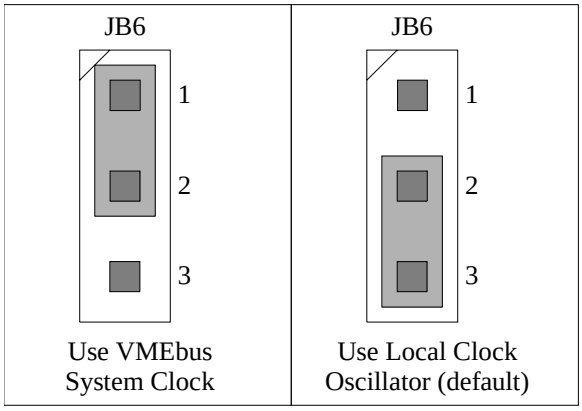

Figure 4-6 System Clock Select

4.3.7 Speed Control

Jumper JB7 and JB8 select the operation mode of the CAN transceivers. The transceivers can work in high speed mode or in slope control mode (low speed).

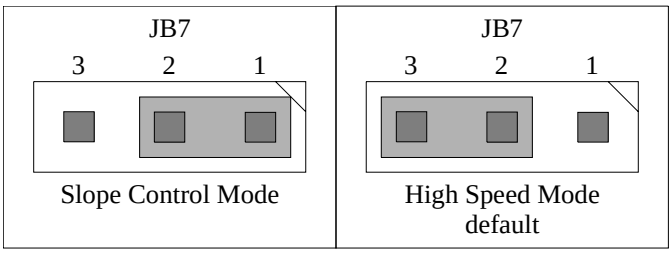

Figure 4-7 Speed Control Channel 0

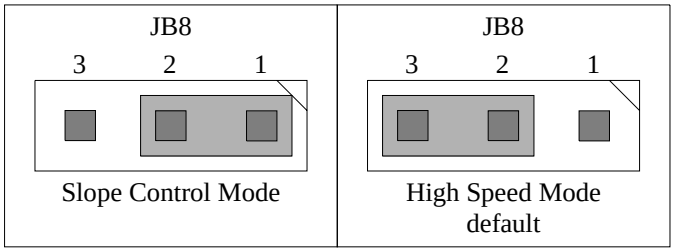

Figure 4-8 Speed Control Channel 1

4.3.8 Physical Interface Input

When the on-board physical interface is used, jumpers must be placed on jumper block JB9 and JB10.

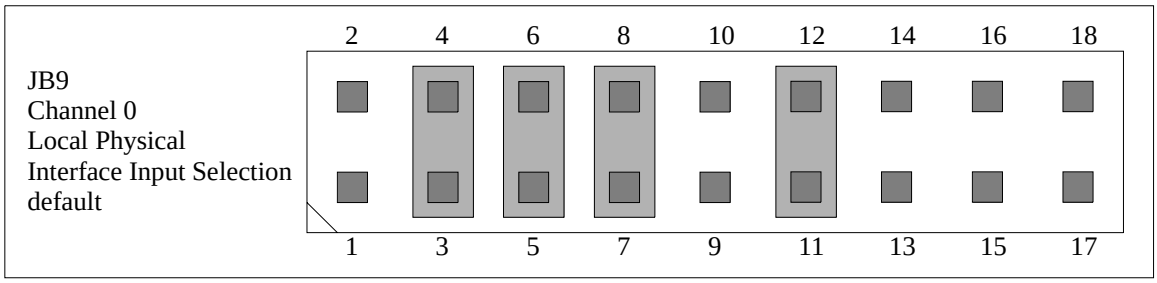

Figure 4-9 Physical Interface Input Channel 0

When a different physical interface is required for channel 0, a mezzanine module can be placed between jumper JB9 and JB11. A more detailed description of the available signals is given in paragraph 4.5.2.

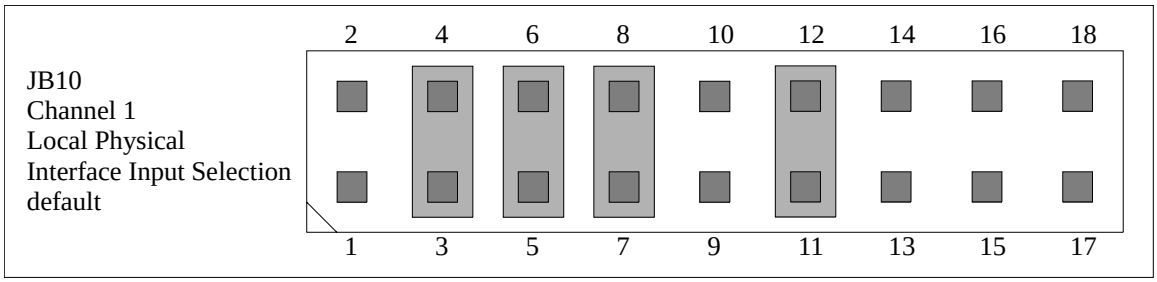

Figure 4-10 Physical Interface Input Channel 1

When a different physical interface is required for channel 1, a mezzanine module can be placed between jumper JB10 and JB12.

4.3.9 Physical Interface Output

When the on-board physical interface is used, jumpers must be placed on jumper block JB11 and JB12.

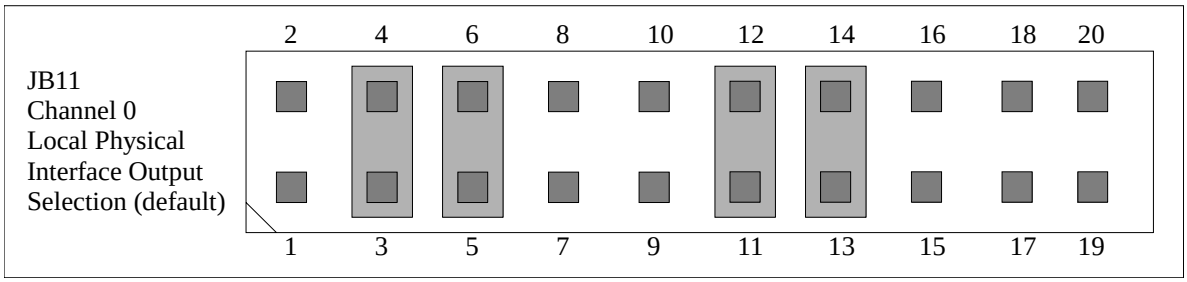

Figure 4-11 Physical Interface Output Channel 0

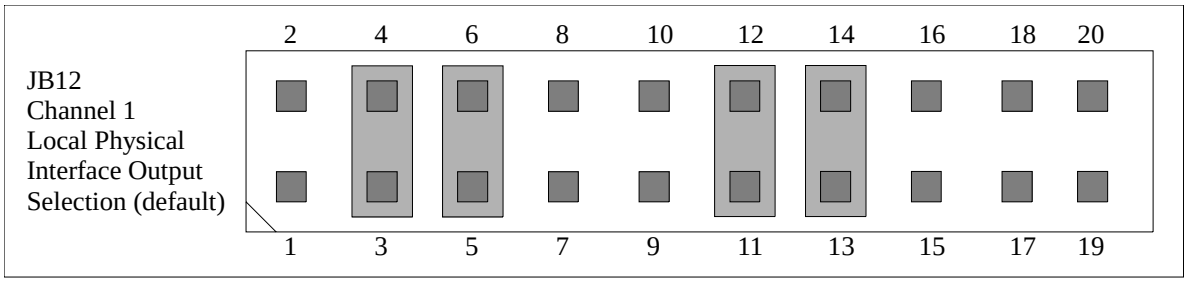

Figure 4-12 Physical Interface Output Channel 1

4.3.10 SRAM Size

The U27-U28 socket pair is used for SRAM devices and may contain the 1 or 4 MBit type SRAMs.

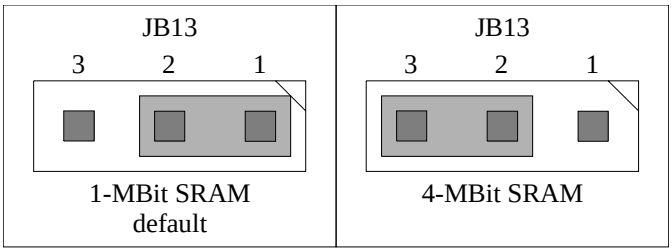

Figure 4-13 SRAM Size Selection

SRAM devices must have a speed of 125 ns (or faster).

4.4 DIP Switch Setting

An 8-position DIP switch setting can be read by the MPU. The switches are numbered from 1 through 8, and each switch can be switched ‘on’ or ‘off’. An ‘on’ position is read as ‘0’ and an ‘off’ position is read as ‘1’.

ON = ’0’

OFF = ’1’

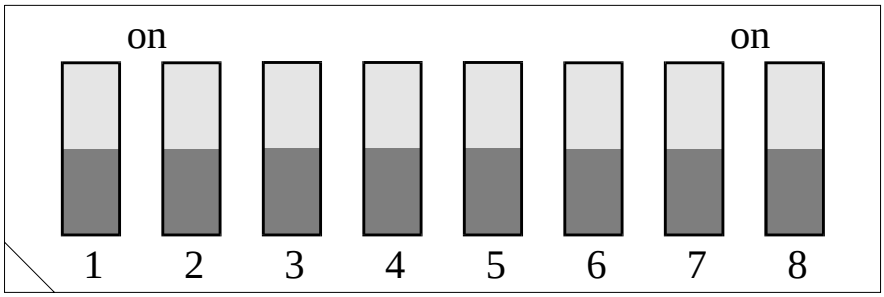

Figure 4-14 DIP Switch Setting

The meaning of the switch settings is defined by the software running on the CC175.

4.5 User Defined Physical Interfaces

The CC175 has two options which allow for user defined physical interfaces.

A DC/DC converter is available on the CC175. The isolated VCC and GND signals can be used on the user defined modules for optical isolation. The DC/DC converter has the following characteristics:

- Output Voltage +5V
- Max. Output Current 360 mA
- Isolation Voltage 500 VDC

4.5.1 VMEbus P2 Transition Modules

The following signals from the controllers are available.

Table 4-2 Signal Descriptions VMEbus P2 Transition Modules

Signal Name Channel[0/1]	Description	Direction
C[0/1]RX0	Input 0 to CAN Controller	To CAN controller
C[0/1]RX1	Input 1 to CAN Controller	To CAN controller
C[0/1]TX0	Output 0 from CAN Controller	To transition
C[0/1]TX1	Output 1 from CAN Controller	To transition
VCC	+5V power supply	To transition
GND	Ground power supply	To transition
VCC DC/DC	Isolated +5V from DC/DC converter	To transition
GND DC/DC	Isolated Ground from DC/DC converter	To transition

4.5.2 Mezzanine Modules

Specific physical interface requirements can be implemented by placing a mezzanine module between the CAN controller and the front connector. This will at the same time bypass the on board physical interface.

The signals from the controllers are available on JB9 and JB10.

Table 4-3 Signal Descriptions JB9 and JB10

Signal Name Channel[0/1]	Description	Direction
C[0/1]RX0	Input 0 to CAN Controller	To CAN controller
C[0/1]RX1	Input 1 to CAN Controller	To CAN controller
C[0/1]TX0	Output 0 from CAN Controller	To mezzanine
C[0/1]TX1	Output 1 from CAN Controller	To mezzanine
C[0/1]VDD2	+5V power supply to input comparator	To CAN controller
SDIO[0/1]	Serial Data Input/Output signal I^2C interface	Bidirectional
SDCLK/ ERRin[0/1]	Serial Data Clock I^2C interface/ ERROR input signal T-CANnector interface	Clock to mezzanine ERROR to CAN controller
ERRrstout[0/1]	Reset Output signal T-CANnector interface	To mezzanine
VCC	+5V power supply	To mezzanine
GND	Ground power supply	To mezzanine
VCC DC/DC	Isolated +5V from DC/DC converter	To mezzanine
GND DC/DC	Isolated Ground from DC/DC converter	To mezzanine
C[0/1]RX1REF	Reference voltage for RX1 input	Not used
JC[0/1]RX0	Input from on board physical interface	Not used
JC[0/1]TX0	Output to on board physical interface	Not used

The signals to the front connector are available on JB11 and JB12.

Table 4-4 Signal Descriptions JB11 and JB12

Signal Name	Description	Direction
CH[0/1]P[1-9]	Direct connection to front connector pin 1 to 9	Bidirectional
VCC DC/DC	Isolated +5V from DC/DC converter	To mezzanine
GND DC/DC	Isolated Ground from DC/DC converter	To mezzanine
CAN[0/1]H	I/O on board physical interface	Not used
CAN[0/1]L	I/O on board physical interface	Not used

See Appendix B for the pin assignments of the mezzanine module connectors.

Appendix D gives the dimensions for the mezzanine modules.

Refer to the 82C200 data sheet for electrical specifications of the CAN Transmit and Receive signals.

The headers for electrical connection of the mezzanine module on the CC175 are the EURODIP SH27-18OZ for JB9 and JB10 and EURODIP SH27-20OZ for JB11 and JB12. The mechanical connection is made by the RICHCO Miniature Support Post MSP-8N.

4.6 Stand Alone Configuration

The CC175 can be used in a stand alone configuration without using a VMEbus backplane. When the CC175 is used outside a VMEbus rack, the following signals must be terminated with a 3.9 kOhm pull-up resistor.

Table 4-5 Signals to be Pulled-up.

P1 Pin Number	Signal
A12	DS1*
A13	DS0*
A14	WRITE*
A16	DTACK*
A18	AS*
A20	IACK*
C11	BERR*
C12	SYSRESET*
C13	LWORD*

Chapter 5

Programming Considerations

5.1 Introduction

This section contains all necessary information for programmers to take full advantage of the features of the CC175 module. The descriptions will include implementation dependent information that cannot be found in the respective data sheets.

This chapter should be used in conjunction with the references given in paragraph 1.5. System programmers are expected to be fully conversant with all the material and have the relevant experience before writing their own system software.

Appendix C shows the Memory map and the I/O map of the CC175 module. It also shows the DUART and CAN Controller Channel 0 and Channel 1 register map.

5.2 Reset

When power is applied to the CC175 module, the on-board power monitor will generate a local reset signal. This reset signal will reset the DUART, the watchdog, the two CAN Controllers and the local processor. After reset, the MPU will fetch its initial program counter and supervisor stack pointer from the EPROM addresses 0-7. The VMEbus SYSRESET* signal has the same effect as a local reset but also resets the VMEbus interrupter. The 68000 reset instruction will only reset the DUART and the two CAN Controllers.

5.3 Watchdog

The on-board watchdog resets the processor when it runs out of program control. After a local reset, the watchdog is idle and becomes active after the first watchdog trigger has been given. To prevent the watchdog from resetting the processor, the watchdog must be triggered every 600 ms. To trigger the watchdog, the OP2 output port of the DUART must be driven to a ‘1’ followed by a ‘0’. This is accomplished by writing $04 to the Set Output Port register ($30001D) followed by writing $04 to the Clear Output Port register ($30001F).

5.4 Local Memory Map

The local EPROM space runs from $000000 through $0FFFFF, where the address locations $000000-$000007 must contain the initial Supervisor Stack Pointer and Program Counter. The local SRAM

space runs from $100000 through $1FFFFF, where the first four bytes are assigned to the mailbox. The mailbox can interrupt or reset the local processor.

The I/O devices are located in 1 MByte memory blocks from $300000-$C00000. The 8-bit peripheral devices only respond at odd addresses. Access to even addresses in the I/O device space will have no effect for write accesses and will return '$FF' on read.

Note that all devices are repeated in the memory map a number of times. The number of times depend on their own size and the space they occupy in the memory map.

Table 5-1 Local Memory Map.

Address	Device
$000000 $0FFFFF	Local EPROM Space 1 MByte (max)
$100000 $1FFFFF	Local SRAM Space 1 MByte (max)
$200000 $2FFFFF	Reserved
$300000 $3FFFFF	Serial Interface
$400000 $4FFFFF	DIP Switch Register
$500000 $5FFFFF	Timer Interrupt / CAN Type / ID7 Register
$600000 $6FFFFF	Module ID
$700000 $7FFFFF	Interrupter
$800000 $8FFFFF	CAN Controller Channel 0
$900000 $9FFFFF	CAN Controller Channel 1
$A00000 $BFFFFF	User LEDs and RSTOUT
$C00000 $FFFFFF	Reserved

5.4.1 EEPROM

The X24C04 is a 512-byte EEPROM with a serial data interface. All address lines are connected to ground. The clock input is programmed via the OP6~ output line of the DUART. The data input line of the EEPROM is connected to the OP5~ output line and the data output from the EEPROM to the IP5~ input line of the DUART.

NOTE: The OP5~ output must be '1' before valid data can be read from the IP5~ input.

A software protocol is used to read and write the contents of the EEPROM, as discussed in the X24C04 data sheet.

The DUART output lines can be individually programmed by writing to the ‘Set Output Port Bits’ register ($30001D) or the ‘Clear Output Port Bits’ register ($30001F). The data written to these registers determine which output lines will be affected. OP5 is affected when writing $20 and OP6 when writing $40. The IP5 input can be read at bit position 5 from the input port register at $30001B.

5.4.2 Shared Memory

The shared memory is a 4-kByte section of the local SRAM and runs from $100000 through $100FFF, as seen by the local processor. VMEbus masters can access this shared SRAM in the VMEbus standard (A24) address space. The access address for VMEbus masters is installed at a 4-kByte boundary using the module ID.

The starting address is calculated as follows: $C00000 + (Module ID x $1000). The next figure shows the address bits used by the VMEbus address comparator.

VMEbus Address Comparator

A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12
’1’	’1’	’0’	’0’	’0’	’0’	’0’	MID4	MID3	MID2	MID1	MID0

Figure 5-1 VMEbus Address Select

5.4.3 Mailbox

The first four memory locations of the shared SRAM are assigned to a mailbox. The mailbox locations 0 and 1 have interrupt capabilities and the mailbox locations 2 and 3 have reset capabilities. When a VMEbus master accesses the interrupt mailbox for write, a level 1 interrupt is generated to the local processor. The local processor uses an autovector to acknowledge this interrupt. When a VMEbus master accesses the reset mailbox for write, the CC175 (including the processor) will receive a hardware reset. Read accesses to the mailbox locations do not activate the reset or interrupt functions.

5.5 Module ID

The module ID register can be read from address $600001. Bit 7 of the module ID register is controlled by the ID7 control register. Note that bit 5 and 6 are always read as ‘11’ and the module ID is given by the least significant five bits.

Module ID Register

	7	6	5	4	3	2	1	0
Address $600001	ID7	’1’	’1’	MID4	MID3	MID2	MID1	MID0
	R	R	R	R	R	R	R	R

Figure 5-2 Module ID Register

5.5.1 ID7 Control Register

The ID7 Control Register is used to control bit 7 of the module ID Register at $600001. Since the contents of the Module ID Register is read during an interrupt acknowledge cycle for VMEbus Interrupts, the ID7 Control Registers allows manipulation of the Status/ID byte. At power up the ID7 bit is cleared to ‘0’. This will set the Status/ID byte to: Module ID + $60.

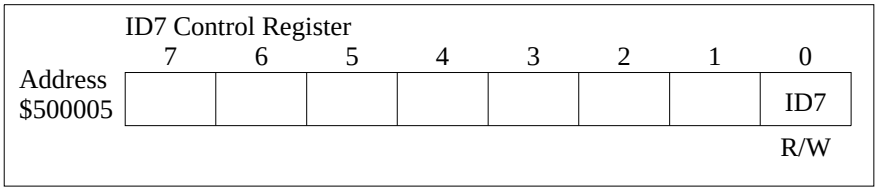

Figure 5-3 ID7 Control Register

5.6 Interrupter

The Interrupter generates an interrupt at one of the seven VMEbus interrupt levels. The interrupt level is selected by jumper JB1. When the VMEbus interrupt handler for this level acknowledges this interrupt, the interrupter (CC175) will generate a Status/ID byte, negate the interrupt line (ROAK - Release on Acknowledge) and responds with DTACK. The Status/ID byte is retrieved from the Module ID register.

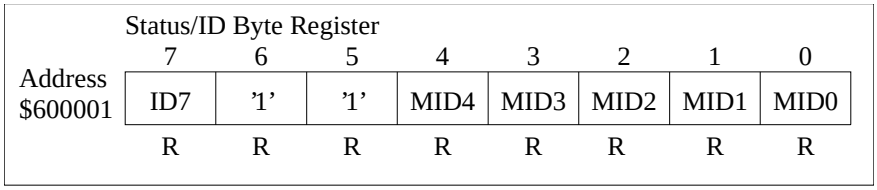

Figure 5-4 Status/ID Byte Register

When the CC175 wants to place a VMEbus interrupt, it should first check that there is no interrupt pending by reading the Interrupt Control Register (ICR) and checking that the ENIRQ bit is ‘0’. Then the ICR is written with the ENIRQ bit ‘1’. Writing a ‘1’ to the ENIRQ bit will actually assert the VMEbus interrupt line. As long as the interrupt is not acknowledged by the VMEbus master, the ENIRQ bit will read as ‘1’. After a corresponding interrupt acknowledge cycle has been generated on the VMEbus, the ENIRQ bit will be cleared (‘0).

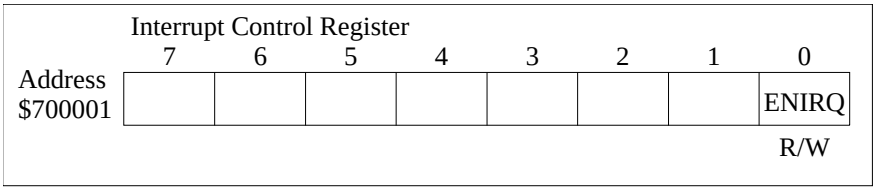

Figure 5-5 Interrupt Control Register

5.7 DUART Serial Interface

The 16 registers of the DUART are located at addresses $300001 through $30001F. The operation of the DUART is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the MPU. The clock frequency of the DUART is 3.6864 MHz. Appendix F shows a detailed register map of the DUART.

Port A is used as an RS-232 interface and supports the signals TxD and RxD on a 9-pin male D-connector at the front panel.
Port B is available via the P2 connector with the TxD, RxD, RTS and CTS signals at TTL level.

The next table shows the usage of the I/O lines of the DUART.

Table 5-2 DUART I/O Lines

Pin Name	Signal Name	Direction	Function
IP0	IP0~	input	ERR from T-CAN Channel 0
IP1	CTSB~	input	Clear to Send Channel B
IP2	IP2~	input	Data Out I^2C Channel 0
IP3	IP3~	input	Data Out I^2C Channel 1
IP4	IP4~	input	ERR from T-CAN Channel 1
IP5	IP5~	input	EEPROM Data
OP0	OP0~	output	Clock I^2C Channel 0
OP1	RTSB~	output	Request to Send Channel B
OP2	WDTRIG~	output	Watchdog Trigger
OP3	OP3~	output	Data In I^2C Channel 0
OP4	OP4~	output	Clock I^2C Channel 1
OP5	OP5~	output	EEPROM Data
OP6	OP6~	output	EEPROM Clock
OP7	OP7~	output	Data In I^2C Channel 1

The DUART input lines can generate a change-of-state interrupt by programming the Auxiliary Control register.

The Output Ports can be programmed to be high (‘1’) or low (‘0’). After Reset, the OPx lines are all ‘1’. The DUART output lines can be individually programmed by writing to the ‘Set Output Port Bits’ register or ‘Clear Output Port Bits’ register. The data written to these registers determine which Output Line(s) will be affected. An output line will be affected when the corresponding data bit is ‘1’.

5.8 CAN Controllers

The operation of the CAN Controllers is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the MPU. Appendix F shows detailed register map of the CAN Controller.

5.8.1 RESET OUT Function

Two RESET OUT signals are available at the CAN Physical Interface. One signal is available at JB9 for CAN Channel 0, the other RESET OUT signal is available at JB10 for CAN Channel 1.

The RESET OUT signal is used in a T-CANnector environment and can be used to indicate error on node.

Setting the RESET OUT bits to zero results in a low RESETOUT signal.

RESETOUT Channel 0 and Channel 1

Address	7	6	5	4	3	2	1	0
$A00007								RSTO1
$B00007								RSTO2

Figure 5-6 RESET OUT

5.9 DIP Switch Register

Address $400001 is used to read the settings of switch SW1. The following figure shows the bit assignments. An ‘on’ position is read as ‘0’ and an ‘off’ position is read as ‘1’.

DIP Switch Register

	7	6	5	4	3	2	1	0
Address $400001	SW8	SW7	SW6	SW5	SW4	SW3	SW2	SW1
	R	R	R	R	R	R	R	R

Figure 5-7 DIP Switch Register

5.10 User LEDs

A total of six User LEDs are available at the CC175 module. User LEDs 1, 2 and 3 are grouped for CAN channel 0 and User LEDs 4, 5 and 6 are grouped for CAN channel 1.

The LEDs will light up when a logic ‘0’ is written to the defined bit position. The LEDs are turned off when these bits are set to ‘1’.

The following figure shows the memory locations of the User LEDs.

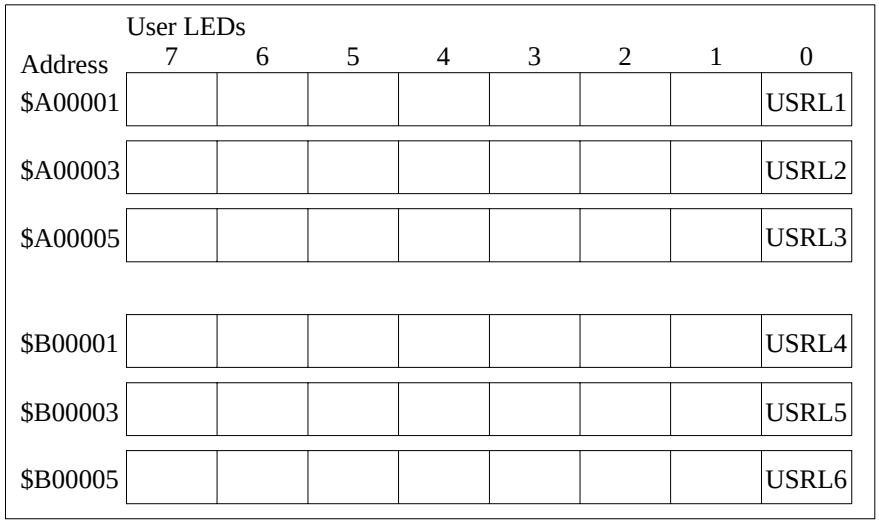

Figure 5-8 User LEDs

5.11 Timer Interrupts

The CC175 has two timer interrupt sources.

5.11.1 Fixed Frequency Timer Interrupts

The CC175 provides a timer which generates an interrupt every 100 µs. The timer interrupts can be enabled/disabled by writing the TIENA bit at the timer interrupt register. Writing this bit to '0' enables the timer and interrupts will be generated every 100 µs. When this bit is set '1', the timer is disabled and no interrupts are generated. The local processor uses an autovector to acknowledge this interrupt.

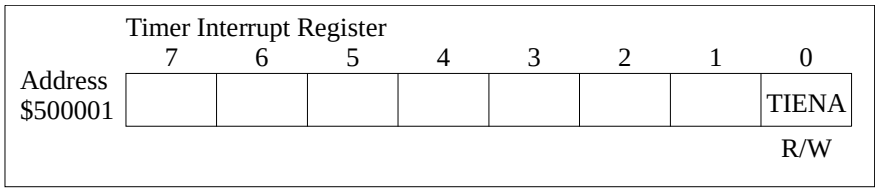

Figure 5-9 Timer Interrupt Register

5.11.2 Programmable Frequency Timer Interrupts

A multi-function programmable 16-bit counter/timer is provided by the SCN68681 DUART. The counter/timer (C/T) operating modes and clock sources are programmed in the ACR[6:4] field.

In the counter mode, the C/T counts down the number of pulses loaded into CTUR and CTLR by the MPU. Upon reaching terminal count 0000_{16}, the counter ready status bit (ISR[3]) is set.

In the timer mode, the C/T generates a square wave with a period of twice the value (in clock periods) of the CTUR and CTLR. In this mode the C/T runs continuously. The counter ready status bit (ISR[3]) is set once each cycle of the square wave.

The counter ready status bit ISR[3] bit can be read and cleared. Interrupts will be generated when the counter ready status bit ISR[3] is a '1' and the interrupt mask register bit IMR[3] is a '1'.

5.12 Bus Time Out

The bus time-out circuit generates a local Bus Error when a device does not respond within 2.4 µs (16 MHz MPU clock).

The bus time-out function is controlled by jumper JB3. During normal operating conditions, no jumper is installed at JB3 and the bus time-out is enabled. A jumper placed at JB3 will disable the bus time-out function.

5.13 Interrupts

The CC175 module handles the following interrupts.The 68000 processor uses automatic vectoring for all these interrupts.

Table 5-3 Interrupt Level Assignments

IRQ Level	Function	Vector Number	Vector Address
1	MAILBOX	$19	$000064
2	CAN Controller Channel 1	$1A	$000068
3	CAN Controller Channel 0	$1B	$00006C
4	DUART	$1C	$000070
5	100 µs Timer Interrupt	$1D	$000074
6	Not Used	$1E	$000078
7	Not Used	$1F	$00007C

Appendix A Block Diagram

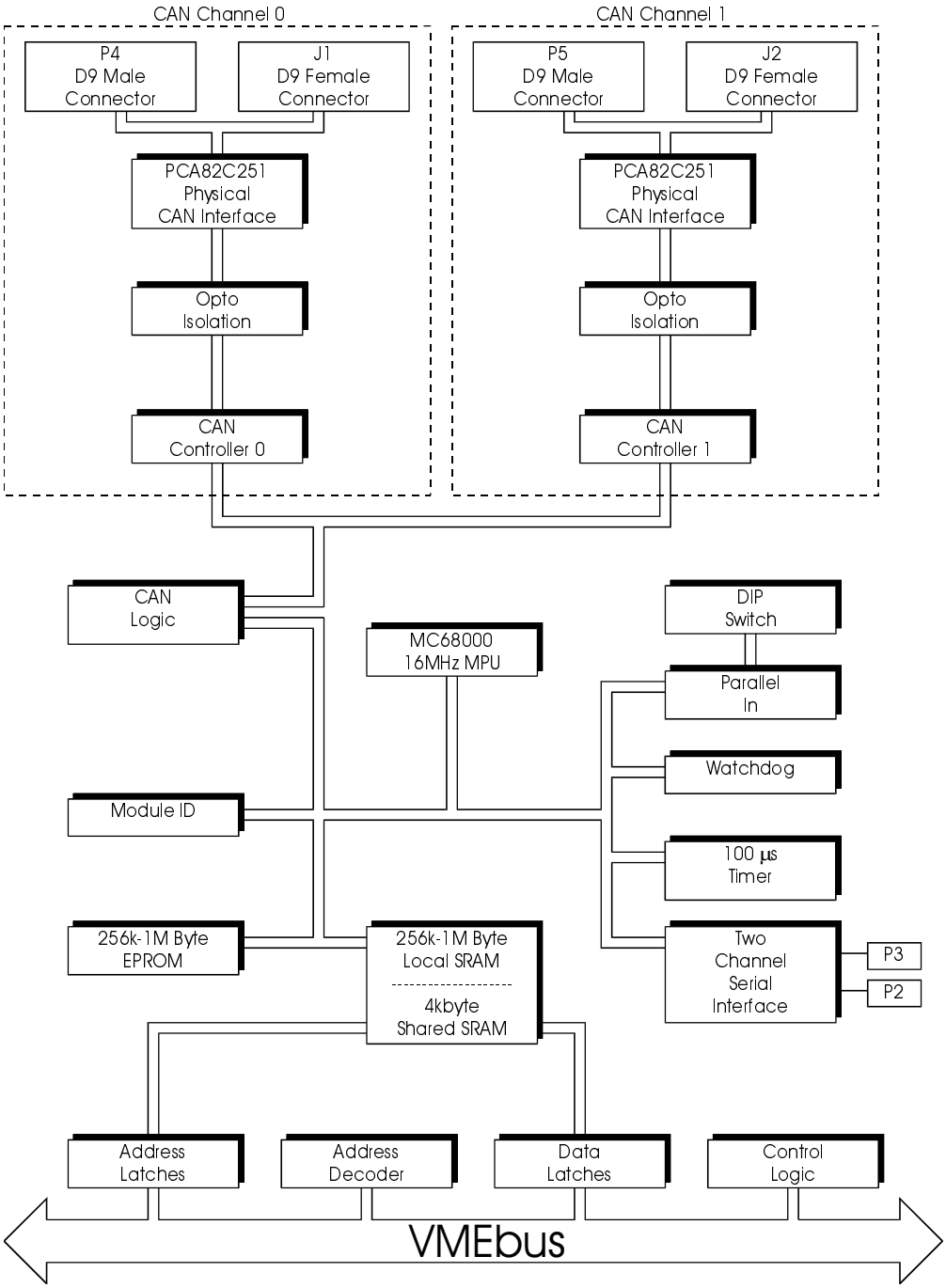

Figure A-1 Block Diagram CC175

Appendix B Connector Assignments

This Appendix identifies the VMEbus P1 and P2 connector, the front connectors P3, P4, P5, J1 and J2 and the mezzanine connectors JB9, JB10, JB11 and JB12.

Table B-1 VMEbus P1

Pin Number	(a) Signal Mnemonic	(b) Signal Mnemonic	(c) Signal Mnemonic
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12V)	(+5V STDBY)	(+12V)
32	+5V	+5V	+5V

Note: Signal mnemonics shown in parenthesis () are not used by the CC175 module.

Table B-2 VMEbus P2

P2 Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1	MIDO		
2	MID1		
3	MID2		
4	MID3		GND
5	MID4		
6			
7	RTSB~		TxDB
8	CTSB~		RxDB
9			
10	C0TX1		C1TX1
11	C0TX0		C1TX0
12	C0RX1		C1RX1
13	C0RX0		C1RX0
14			
15	VCC		VCC
16	GND		GND
17			
18			
19			
20	EXTVCC		EXTVCC
21	EXTGND		EXTGND
22			
23	CH1P9		CH0P9
24	CH1P8		CH0P8
25	CH1P7		CH0P7
26	CH1P6		CH0P6
27	CH1P5		CH0P5
28	CH1P4		CH0P4
29	CH1P3		CH0P3
30	CH1P2		CH0P2
31	CH1P1		CH0P1
32			

Table B-3 Serial I/O Channel A, RS-232 Interface P3

P3 Pin Number	CC175 Signal Mnemonic	Direction
2	RDA	IN
3	TDA	OUT
5	GND	
7	RTSA (GND)	OUT

Table B-4 Channel 0 CAN Interface

J1 Pin Number	P4 Pin Number	CC175 Signal Mnemonic	Default CAN Signal Connected
1	1	CH0P1	(No Connection)
2	2	CH0P2	CAN0_L
3	3	CH0P3	EXTGND
4	4	CH0P4	(No Connection)
5	5	CH0P5	(No Connection)
6	6	CH0P6	EXTGND
7	7	CH0P7	CAN0_H
8	8	CH0P8	(No Connection)
9	9	CH0P9	(No Connection)

Table B-5 Channel 1 CAN Interface

J2 Pin Number	P5 Pin Number	CC175 Signal Mnemonic	Default CAN Signal Connected
1	1	CH1P1	(No Connection)
2	2	CH1P2	CAN1_L
3	3	CH1P3	EXTGND
4	4	CH1P4	(No Connection)
5	5	CH1P5	(No Connection)
6	6	CH1P6	EXTGND
7	7	CH1P7	CAN1_H
8	8	CH1P8	(No Connection)
9	9	CH1P9	(No Connection)

Table B-6 JB9 and JB10 Mezzanine Input

JB9 Pin Number	CC175 Signal Mnemonic	JB10 Pin Number	CC175 Signal Mnemonic
1	VCC	1	VCC
2	VCC	2	VCC
3	C0RX0	3	C1RX0
4	JC0RX0	4	JC1RX0
5	C0RX1	5	C1RX1
6	C0RX1REF	6	C1RX1REF
7	C0TX0	7	C1TX0
8	JC0TX0	8	JC1TX0
9	C0TX1	9	C1TX1
10	(No Connection)	10	(No Connection)
11	C0VDD2	11	C1VDD2
12	VCC	12	VCC
13	SDIO Channel 0	13	SDIO Channel 1
14	(No Connection)	14	(No Connection)
15	SDCLK/ERRin Channel 0	15	SDCLK/ERRin Channel 1
16	ERRrstout Channel 0	16	ERRrstout Channel 1
17	GND	17	GND
18	GND	18	GND

Table B-7 JB11 and JB12 Mezzanine Output

JB11 Pin Number	CC175 Signal Mnemonic	JB12 Pin Number	CC175 Signal Mnemonic
1	(No Connection)	1	(No Connection)
2	CH0P1	2	CH1P1
3	CAN0_L	3	CAN1_L
4	CH0P2	4	CH1P2
5	EXT GND	5	EXT GND
6	CH0P3	6	CH1P3
7	(No Connection)	7	(No Connection)
8	CH0P4	8	CH1P4
9	(No Connection)	9	(No Connection)
10	CH0P5	10	CH1P5
11	EXT GND	11	EXT GND
12	CH0P6	12	CH1P6
13	CAN0_H	13	CAN1_H
14	CH0P7	14	CH1P7
15	(No Connection)	15	(No Connection)
16	CH0P8	16	CH1P8
17	(No Connection)	17	(No Connection)
18	CH0P9	18	CH1P9
19	EXT VCC	19	EXT VCC
20	EXT VCC	20	EXT VCC

Appendix C Memory and I/O Map

Table C-1 Local Memory Map

Address Range	Device
$000000 - $03FFFF	Local EPROM Space (1 Mbit Devices)
$000000 - $07FFFF	Local EPROM Space (2 Mbit Devices)
$000000 - $0FFFFF	Local EPROM Space (4 Mbit Devices)
$100000 - $100FFF	4 kbyte Shared SRAM Space
$101000 - $13FFFF	Local SRAM Space (1 Mbit Devices)
$101000 - $1FFFFF	Local SRAM Space (4 Mbit Devices)
$200000 - $2FFFFF	Reserved
$300000 - $30001F	Serial Interface (DUART)
$300020 - $3FFFFF	DUART Repeated in Memory Map
$400000 - $400001	DIP Switch Register
$400002 - $4FFFFF	Register Repeated in Memory Map
$500000 - $500001	Timer Interrupt
$500002 - $500003	CAN Controller Type
$500004 - $500005	ID7 Control Register
$500008 - $5FFFFF	Registers Repeated in Memory Map
$600000 - $600001	Module ID
$600002 - $6FFFFF	Module ID Repeated in Memory Map
$700000 - $700001	Interrupt Control Register
$700002 - $7FFFFF	ICR Repeated in Memory Map
$800000 - $80003F	CAN Controller Channel 0
$800040 - $8FFFFF	CAN Controller 0 Repeated in Memory Map
$900000 - $90003F	CAN Controller Channel 1
$900040 - $9FFFFF	CAN Controller 1 Repeated in Memory Map
$A00000 - $A00001	User LED 1 (green)
$A00002 - $A00003	User LED 2 (yellow)
$A00004 - $A00005	User LED 3 (red)
$A00006 - $A00007	RESET OUT Channel 0
$A00008 - $AFFFFF	Registers Repeated in Memory Map
$B00000 - $B00001	User LED 4 (green)
$B00002 - $B00003	User LED 5 (yellow)
$B00004 - $B00005	User LED 6 (red)
$B00006 - $B00007	RESET OUT Channel 1
$B00008 - $BFFFFF	Registers Repeated in Memory Map
$C00000 - $FFFFFF	Reserved

Table C-2 VMEbus Memory Map

Address Range	Device
$Cxx000 - $Cxx001	Shared RAM Mailbox with Interrupt Function
$Cxx002 - $Cxx003	Shared RAM Mailbox with Reset Function
$Cxx004 - $CxxFFF	Shared RAM

The address of the Shared RAM in the VMEbus memory map depends on the Module ID value. The Module ID replaces ‘xx’ in the memory map of table C-2.

Table C-3 DUART Register Map

Address	Read Register Name	Write Register Name
$300001	Mode Register A (MR1A, MR2A)	Mode Register A (MR1A, MR2A)
$300003	Status Register A (SRA)	Clock Select Register A (CSRA)
$300005	*Reserved*	Command Register A (CRA)
$300007	Rx Holding Register A (RHRA)	Tx Holding Register A (THRA)
$300009	Input Port Change Reg. (IPCR)	Auxiliary Control Register A (ACR)
$30000B	Interrupt Status Register (ISR)	Interrupt Mask Register (IMR)
$30000D	Counter/Timer Upper (CTU)	Counter/Timer Upper Reg. (CTUR)
$30000F	Counter/Timer Lower (CTL)	Counter/Timer Lower Reg. (CTLR)
$300011	Mode Register B (MRB1, MR2B)	Mode Register B (MR1B, MR2B)
$300013	Status Register B (SRB)	Clock Select Register B (CSRB)
$300015	*Reserved*	Command Register B (CRB)
$300017	Rx Holding Register B (RHRB)	Tx Holding Register B (THRB)
$300019	Interrupt Vector Register (IVR)	Interrupt Vector Register (IVR)
$30001B	Input Port Register (IPR)	Output Port Config. Reg. (OPCR)
$30001D	Start Counter Command	Set Output Port Bits Command
$30001F	Stop Counter Command	Reset Output Port Bits Command

Table C-4 82C200 CAN Controller Register Map

Address Channel 0	Address Channel 1	Register Name
$800001	$900001	Control Register
$800003	$900003	Command Register
$800005	$900005	Status Register
$800007	$900007	Interrupt Register
$800009	$900009	Acceptance Code Register
$80000B	$90000B	Acceptance Mask Register
$80000D	$90000D	Bus Timing Register 0
$80000F	$90000F	Bus Timing Register 1
$800011	$900011	Output Control Register
$800013	$900013	Test Register
$800015	$900015	Transmit Buffer Identifier
$800017	$900017	Transmit Buffer RTR Data Length
$800019 $800027	$900019 $900027	Transmit Buffer Data (8 bytes)
$800029	$900029	Receive Buffer Identifier
$80002B	$90002B	Receive Buffer RTR Data Length
$80002D $80003B	$90002D $90003B	Receive Buffer Data (8 bytes)
$80003D	$90003D	Clock Divider

Appendix D Mechanical Specifications

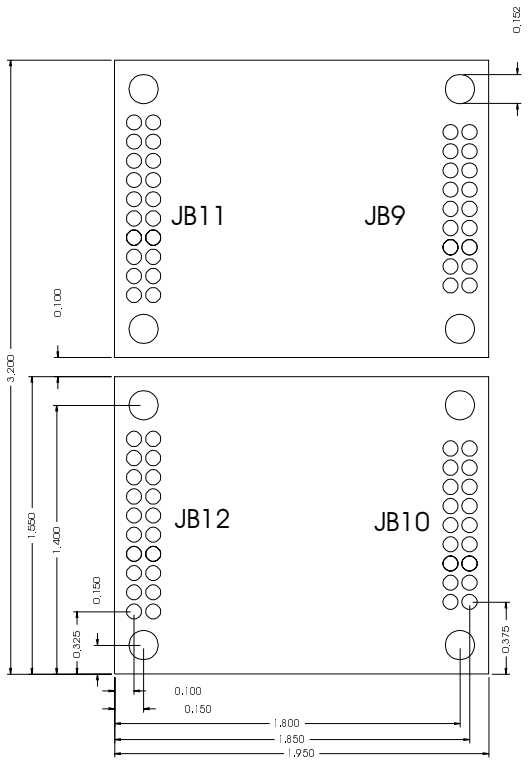

Figure D-1 Mechanical Specification Mezzanine Module

All dimensions are shown in inches.

Appendix E Photo CC175 Board

Placeholder

Figure E-1 Photo CC175 Board