Technical Manual CC433
12 Channel Incremental Encoder Interface With Isolated Inputs
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Table of Contents

List of Figures

List of Tables

Chapter 1

General Information

1.1 Introduction

This manual provides general information, instructions for preparation for use, installation instructions and theory of operation for the CC433 Incremental Encoder Interface for the VMEbus.

The VMEbus board can determine the rotation or translation, direction and displacement of up to twelve mechanical devices or axis, based on two input signals from transducers in quadrature.

1.2 Features

The features of the CC433 module include:

VMEbus

- VMEbus slave interface (A16;D16)
- Flexible base address selection
- Interrupter I(1-7)DYN
- Selectable address modifier decoding
- Occupies 256 memory locations

Channel Grouping

- Four independent groups of 3 channels
- Each group of channels shares:
- a D25 front panel connector
- an interrupt level
- an interrupt vector
- a fault detect delay register
- a counter mode register
- a device reset register
- two CF32006 devices in a master/slave configuration

Channel Configuration

- Two quadrature inputs
- One index input
- One digital input
- Cable fault detection on all inputs
- One 32 bit up/down counter

- Direct digital input register
- Change of state detection circuit
- Interrupt mask register
- Enable index register
- Index status register

Input Signal Configuration

- Each input is galvanically isolated from the system
- Each input is galvanically isolated from any other input
- Differential or single ended configuration possible

1.3 General Description

The CC433 12 Channel Incremental Encoder Interface module is a VMEbus slave module. The module decodes the address lines A1 to A15 and responds when receiving the address modifier codes $29 and/or $2D (short supervisory/non-privileged I/O access). The module appears to the system as 256 byte locations which can be placed on any 256 byte boundary in the 64 kbyte short I/O space.

The module consists of 12 input channels with four differential inputs each. The channels are grouped in four independent groups. Each group is based upon two CF32006 triple incremental encoder counters and has its own synchronization and control logic.

The differential inputs are optically isolated from the synchronization circuitry. An isolation of 500 V is maintained between any two inputs and between any input and the system.

Each channel has two quadrature input signals, one index input and one digital input. The index input may reset the corresponding counter and/or generate an interrupt. The polarity of the index input is programmable.

The index and the digital input create a two bit digital input channel. A change of a digital input line of a channel can be detected and may generate an interrupt when this change is detected. The interrupter is a MC68153 Bus Interrupter Module (BIM) which has a software programmable interrupt level, interrupt vector and interrupt mask register for each of the four channel groups.

The differential input signals are continuously monitored to check whether a proper differential signal is applied to the inputs. When a non-differential signal is detected, due to missing connections or electrical shorts, cable fault bits are set in registers which can result in an interrupt to the VMEbus being asserted.

1.4 Ordering Information

The following versions of the CC433 are available:

Table 1-1 Ordering Information

Module	Number of Groups	Number of Channels
CC433-3	1	3
CC433-6	2	6
CC433-9	3	9
CC433-12	4	12

1.5 Related Documents

The following manuals are also relevant:

Table 1-2 List of Documents

Document Title	Published By
The VMEbus Specification Manual (ANSI/IEEE 1014-1987, IEC 821 and 927	VITA
CF32006 Triple Incremental Encoder Interface Data sheet	Texas Instruments

Chapter 2

Specifications

2.1 Introduction

This chapter provides a summary of the components, and a detailed specification of the module. The CC433 is a highly-integrated and high-performance VMEbus incremental encoder interface module based on the CF32006 Triple Incremental Encoder Interface.

2.2 Components Used

The CF32006 Triple Incremental Encoder Interface Chip consists of three identical incremental encoder interface circuits. This encoder interface can be configured into one of three operating modes: direction discrimination with five modes of counter incrementation, pulse width measurement, and frequency measurement.

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microprocessor system. An interrupt request from any device is routed to the MC68153, and the BIM handles all interfacing to the VMEbus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handle all timing.

Two Field Programmable Gate Array (FPGA) devices are used to monitor and synchronise the differential input signals to the CF32006 devices. The FPGA devices also contain all the group functions that are not provided by the CF32006 and the MC68153 devices.

2.3 VMEbus Options

Data Transfer Options

- DTB Slave A16;D16,D8: RMW,ADO
- Selectable AM codes: $29,$2D

Interrupter Options

- I(1,2,3,4,5,6,7)DYNAMIC INTERRUPTER
- Release on Acknowledge(ROAK)
- Release on Register Access(RORA)
- D08(O) Status/ID byte

Power Options

- 1.5 A Typical (2 A Maximum) at +5 Vdc

Physical Configuration Options

- Double-Height Eurocard format
- Single-Width front panel

Environmental Requirements

- Operating Temperature: 0-70 degrees C
- Maximum operating humidity: 90%

2.4 Input Specifications

Input Signals

- Differential Mode Receivers conform to RS-422-A
- Maximum Differential Voltage: 5 V
- Single ended input signals are possible
- Detection of non-differential signal on all inputs

Input Frequency

- Maximum Frequency on all inputs: 1 Mhz

Insulation

- Input Signal to System:

  Optocoupler HCPL-2631 Recognized under the Component Program of U.L.(File No. E55361) for Dielectric Withstand Proof Test Voltages of 2500 VAC, 1 Minute, RH $\leq 50\%$, T_A = 25 °C

Chapter 3

Functional Description

3.1 Introduction

This chapter provides an overview of the CC433 module, and a detailed description of each functional section. The block diagram of the module is shown in Appendix A.

3.2 Group Description

The twelve available input channels on the CC433 are divided into four identical, independent groups: Group A to Group D. Each group is built up around two cascaded CF32006 triple incremental encoder interface circuits. The following paragraphs describe the functions of a single group.

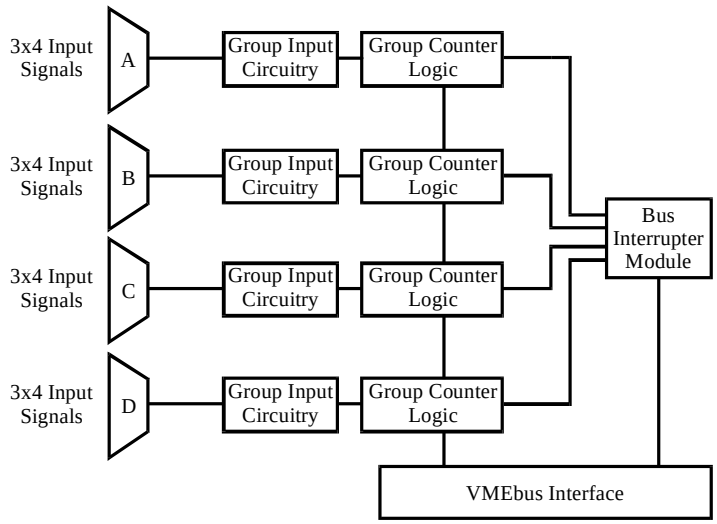


Figure 3-1 Input Groups

3.2.1 Group Input Circuit

Figure 3-2 shows a function diagram of the input circuit for each group on the CC433.

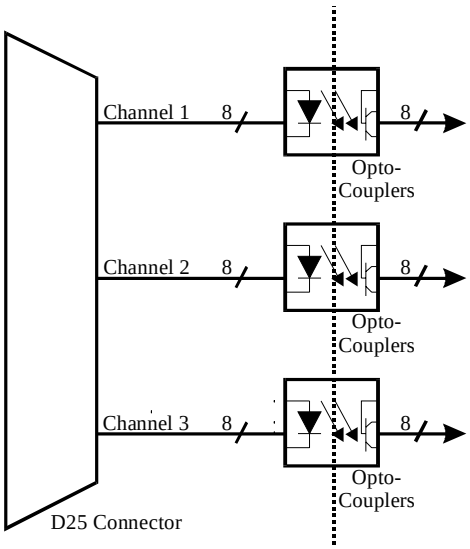


Figure 3-2 Group Input Circuit

The input signals are passed via a D25 male connector to the CC433. Each D25 connector receives the signals for three channels. Opto-couplers are used for galvanic isolation between the differential signals and the system. Each opto-coupler input circuit meets the requirements of the RS-422-A standard and converts the differential input signal to a standard TTL signal. The ‘minus’ input can be connected to ground, to let the ‘plus’ input accept a single ended input signal.

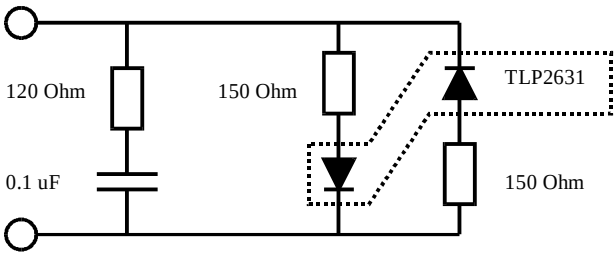


Figure 3-3 Input Signal Termination

All input signals are received using the circuit as depicted in Figure 3-3. The combination of the parallel resistors, diodes and the series capacitor give an input impedance that approximates a nominal termination value of 120 Ohm. Differential input signals are properly terminated by this input circuitry and no additional termination is required.

3.2.2 Channel Description

Each channel of the CC433 consists of four signals: two quadrature signals, one index signal and one digital Input signal.

The quadrature signals are used to supply information from the field to the control system. The information is translated by the encoder circuits into numeric values. The logic levels of the quadrature signals

and their relative edges will result in an increment or decrement function of the encoder counters, depending on the current operating mode of the encoder circuits.

The index signal can be used to reset the encoder counters and generate an interrupt to the VMEbus. The digital Input signal can serve several functions within the working environment, and can also be used to generate an interrupt to the VMEbus. The interrupt capability of both signals is fully described in the next section.

3.2.3 Interrupt Capability

Each group on the CC433 can generate an interrupt request, independent of the other groups. Possible sources for interrupts are the digital Input signal, the index signal, the 32 bit counter carry and borrow signals and the fault detection circuit signals.

A Compare State Register is implemented on the CC433 to detect events on the digital Input signal and the index signal. The next figure shows how this circuit is functionally implemented.

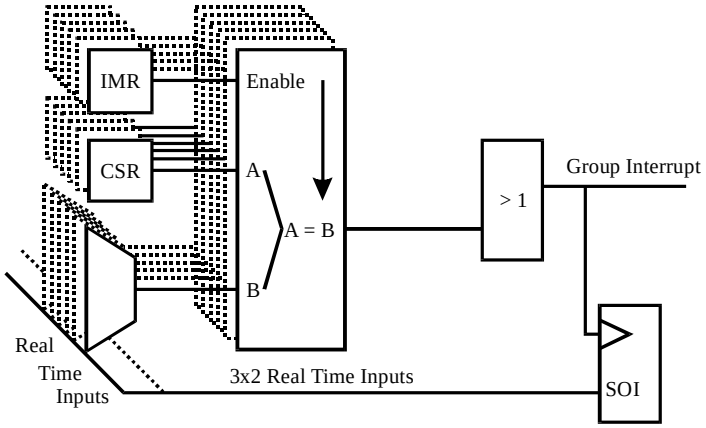


Figure 3-4 Compare State Circuit

Several registers are implemented on the CC433 for generating and controlling of the interrupt capability. Each channel has the following interrupt control/status registers:

- Direct Input Register
- Compare State Register (CSR)
- State On Interrupt Register (SOI)
- Interrupt Mask Register (IMR)

To detect a change in the input lines, the comparator must compare the real time input lines with a copy of the previous state of the input lines. A copy is made of the current state of the input lines by reading the Direct Input Register, and this data should be written into the Compare State Register. An interrupt will be generated as soon as the real time input changes and the corresponding input is enabled in the Interrupt Mask Register. The current states of the index and digital Input signals are saved in the State On Interrupt Register register at the time of the interrupt request. Each group has its own interrupt request signal to the Bus Interrupter Module.

Further detailed programming considerations are given in chapter 5.

3.2.4 Group Operation Modes

The CF32006 encoder circuit can work in eight different modes. The mode of operation is programmed into the encoder circuit by writing the mode number to the Group Mode Register of the specific group.

Note: There is only one mode register available per group so the three channels in one group share the same mode.

3.2.5 Mode Description

There are eight different modes of operation on a CF32006 encoder circuit: one counter mode, five direction discriminator modes, one mode to measure a pulse width, and one mode to measure the frequency of a signal.

3.2.5.1 Counter Mode 0

Using the cascaded configuration (32 bit counter), the Most Significant Counter (MSC) must operate in the counter mode. With this mode, the MSC reacts only on the up and/or down pulse from the Least Significant Counter (LSC). The MSC device is hardwired to this mode.

Note: The LSC should not be programmed in the counter mode, since this will not result in any reaction when quadrature signal levels are changed.

3.2.5.2 Direction Discriminator Modes 1 to 5

A channel's quadrature signals Ua1 and Ua2 identify forward or backward directions. If Ua1 leads Ua2, the forward direction is indicated and the counter will count up. If Ua1 lags Ua2, the reverse direction is indicated and the counter will count down.

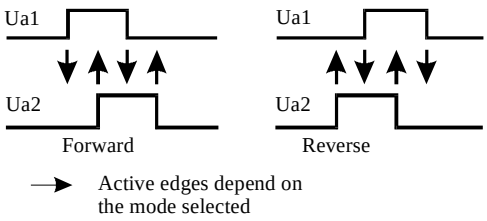


Figure 3-5 Direction Discriminator Modes

The next figures show the five available direction discriminator modes, and the reaction of the encoder circuit to these modes.

Figure 3-6 shows the waveforms which force the encoder circuit to generate pulses for counting up.

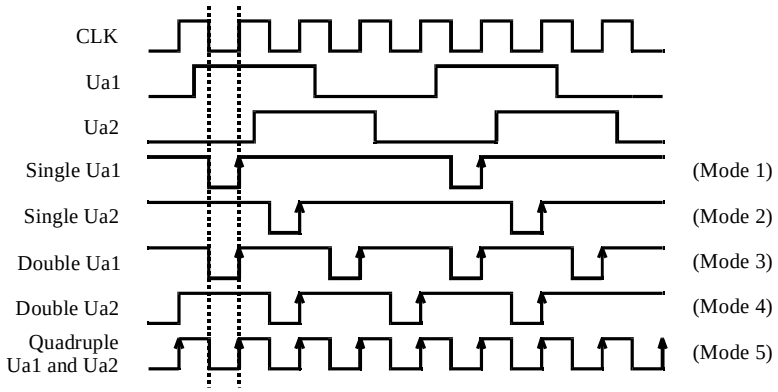


Figure 3-6 Direction Discriminator Up Clock

Figure 3-7 shows the waveforms which must be used for counting down.

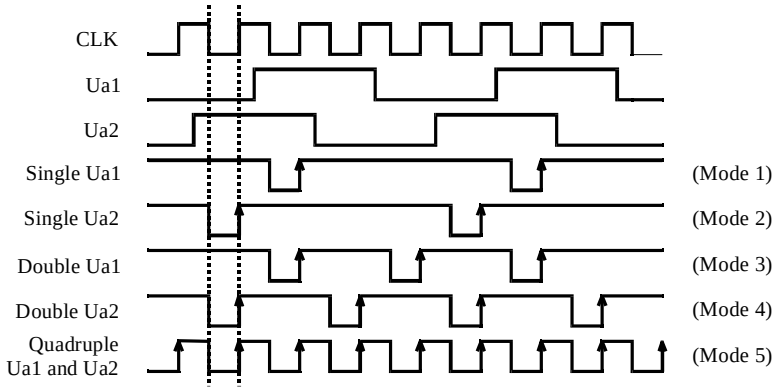


Figure 3-7 Direction Discriminator Down Clock

3.2.5.3 Pulse Width Measurement Mode 6

In this mode Ua1 gates the pulse width to be measured. When synchronized with the clock edge after a low to high transition in Ua1, counting begins at the input clock frequency of 10 MHz. Similarly, when synchronized with the clock edge after a high to low transition of Ua1, counting is disabled. The value in the counter is stored in the Channel Counter Output Register and the counter is cleared. If Ua2 is held high the counter will count up, and if Ua2 is held low the counter will count down.

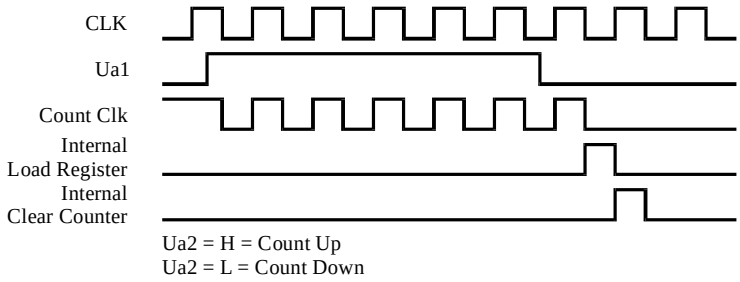


Figure 3-8 Pulse Width Measurement

3.2.5.4 Frequency Measurement Mode 7

In Mode 7, Ua1 carries the signal of unknown frequency to be measured, and Ua2 is a gate signal of known width. A low to high transition of the Ua2 signal enables counting at the frequency of Ua1. When the gate Ua2 goes low, counting is disabled and the value is stored again in the Channel Counter Output Register, and the counter is cleared.

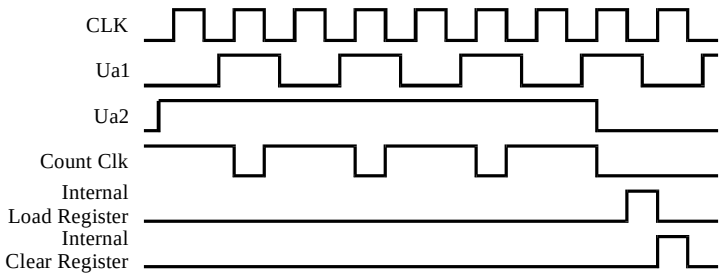


Figure 3-9 Frequency Measurement

3.2.6 Reset Operation

A total reset is initiated by a write access to the Group Reset Register. Depending on the state of the quadrature signals, the counters can be cleared, or set to +1 or -1. To avoid this count error (+1 or -1) after the reset, the Ua1n and the Ua2n inputs should be held to the values indicated in table 3-1 during and just after the write access. It is recommended to check if the counters are cleared after the group reset.

Table 3-1 Reset Operation

Mode	Ua1n	Ua2n
0	X	X
1 to 5	H	H
6 to 7	L	L

3.3 Bus Interrupt Module

The Bus Interrupter Module on the CC433 generates interrupt requests to the VMEbus and handles interrupt acknowledge cycles.

For each group on the CC433, the interrupt capability is enabled/disabled by writing to the corresponding control registers of the BIM. In addition, each group has its own interrupt vector, which is used during the interrupt acknowledge cycle.

Chapter 4

Installation Procedures

4.1 Introduction

This chapter provides hardware preparation and installation instructions for the CC433 Incremental Encoder Module.

4.2 Installation

The module is shipped in an anti-static container which protects it against static electricity. When the module is unpacked, avoid touching areas of integrated circuitry to prevent static discharge from damaging the circuits.

The module can be used in VMEbus compatible systems and can be configured to suit many applications.

The pin definition of the VMEbus P1, P2 and the I/O connectors P3, P4, P5 and P6 can be found in Appendix E.

NOTE: ENSURE THAT THE POWER IS TURNED OFF BEFORE INSERTING OR EXTRACTING THE CC433 MODULE IN OR FROM THE SYSTEM BACKPLANE.

4.3 Address Selection

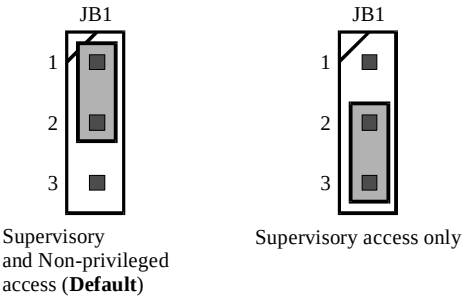
The CC433 module occupies 256 memory locations in the Short I/O space. The base address can be installed on any 256 byte boundary using hex switches SW1 and SW2. SW1 is used to set the Most significant nibble of the base address (A15-A12). SW2 is used to set the Least significant nibble of the base address (A11-A8).

4.4 Jumper Settings

The jumper setting discussed in the following section is illustrated as seen from the component side with both VMEbus connectors downwards.

4.4.1 Jumper JB1 - Access Mode

When the connection is made between pins 1 and 2 of JB1, the module will respond to both Supervisory AM code $2D and non privileged AM code $29. When pins 2 and 3 are connected, the module will respond only to the Supervisory AM code $2D.



Supervisory and Non-privileged access (**Default**)

Supervisory access only

Figure 4-1 Jumper JB1 - Access Mode

4.5 Input/Output Connections

The inputs for each channel are made available at the front panel P3, P4, P5 and P6 D-25 male connectors. The next table shows the connector assignments for each channel.

Table 4-1 Channel Connector Assignments

Connector	Group	Channels
P3	A	1-3
P4	B	4-6
P5	C	7-9
P6	D	10-12

Appendix E shows the connector pin assignments for the CC433 module.

Chapter 5

Operating Instructions

5.1 Introduction

This chapter provides operating instructions for the CC433 module and also all necessary information for system programmers to take full advantage of the features of the module. The descriptions will include implementation dependent programming information that can not be found in data sheets.

The memory map of the CC433 is divided into four identical sections. Each part, or group, contains the registers of three channels.

Table 5-1 Global Memory Map

Group Offset	Description
$00	Group A Registers - Channels 1, 2 and 3
$40	Group B Registers - Channels 4, 5 and 6
$80	Group C Registers - Channels 7, 8 and 9
$C0	Group D Registers - Channels 10, 11 and 12

5.2 Device Group Registers

Each device group consists of three sets of channel registers and several shared group registers. Each group has its own set (master/slave) of two CF32006 devices.

Table 5-2 Device Group Registers

Channel Offset	Description
$00	Channel Registers
$10	Channel Registers
$20	Channel Registers
$31	Group Fault Delay Register
$33	Group Mode Register
$37	Group Reset Register
$3B	Group BIM Control Register
$3F	Group BIM Vector Register

5.2.1 Channel Registers

A channel consists of a set of registers described in the following paragraphs. The actual VMEbus address of the registers can be calculated by adding the Group Offset and the Channel Offset to the board base address.

Table 5-3 Channel Registers

Register Address	Description
$00	Channel Counter Registers
$05	Enable Index Register
$07	Index Status Register
$09	Direct Input Register
$0B	Compare State Register
$0D	State On Interrupt Register
$0F	Interrupt Mask Register

5.2.1.1 Channel Counter Registers

When one byte is read, the encoder chip generates a load output latch pulse for the four bytes of the Counter register. From that time until the next system reset, the load output latch pulse will only be generated during a read operation if this same byte is read. Special care should be taken if reading individual bytes to ensure that these operations are always performed in the same order.

Table 5-4 Channel Counter Registers

Channel Offset Read/Write	7	6	5	4	3	2	1	0
$00	C31	C30	C29	C28	C27	C26	C25	C24
$01	C23	C22	C21	C20	C19	C18	C17	C16
$02	C15	C14	C13	C12	C11	C10	C9	C8
$03	C7	C6	C5	C4	C3	C2	C1	C0

5.2.1.2 Enable Index Register

This registers is used to set whether an index pulse will reset the counter and at which level this index pulse will be active.

Table 5-5 Enable Index Register

Channel Offset Read/Write	7	6	5	4	3	2	1	0
$05							LVLIND	EIND

EIND When EIND=1, an index pulse will reset the counter.
When EIND=0, the index pulse is masked and will not reset the counter.

LVLIND When LVLIND=0, a ‘1-0-1’ pulse on the index input will clear the counter, if enabled using EIND.
When LVLIND=1, a ‘0-1-0’ pulse on the index input will clear the counter, if enabled using EIND.

After a SYSRESET these bits are cleared.

Note: The state of the EIND bit does not affect the interrupt capability of the index input.

5.2.1.3 Index Status Register

This register gives the status of several events that can occur.

Table 5-6 Index Status Register

Channel Offset Read Only	7	6	5	4	3	2	1	0
$07					CAR	BOR	DIS	INDS

CAR This bit is set when a 32 bit carry has occurred. It signals a 32 bit counter over flow.

BOR This bit is set when a 32 bit borrow has occurred. It signals a 32 bit counter under flow.

DIS This bit is set when the digital input DI has been active.

INDS When INDS=1, an index pulse has occurred. It can only be set when the EIND bit in the Enable Index Register is set.

All bits are cleared after the Index Status Register has been read.

5.2.1.4 Direct Input Register

This register provides the current state of the input signals.

Table 5-7 Direct Input Register

Channel Offset Read Only	7	6	5	4	3	2	1	0
$09	F_Ua2	F_Ua1	F_DI	F_IND	Ua2	Ua1	DI	IND

F_Ua2 This bit is set when a non-differential input signal is detected on the Ua2 input. This bit will stay set until the Direct Input Register is read.

F_Ua1 This bit is set when a non-differential input signal is detected on the Ua1 input. This bit will stay set until the Direct Input Register is read.

F_DI This bit is set when a non-differential input signal is detected on the digital input. This bit will stay set until the Direct Input Register is read.

F_IND This bit is set when a non-differential input signal is detected on the index input. This bit will stay set until the Direct Input Register is read.

Ua2, Ua1 These bits directly reflect the state of the channel's quadrature signals.

DI This bit directly reflects the state of the channel's digital input signal.

IND This bit directly reflects the state of the channel's index input signal.

5.2.1.5 Compare State Register

This register specifies the levels the digital input signals will be compared to.

Table 5-8 Compare State Register

Channel Offset Read/Write	7	6	5	4	3	2	1	0
$0B							CDI	CIND

When the digital inputs differ from the values of CDI and CIND written in this register, an interrupt can be generated and a sample of the digital inputs is made in the State On Interrupt Register.

After an interrupt is generated due to a change of state, a write access to the Compare State Register must be performed before another interrupt can be generated in the specific group. The write access to the Compare State Register will clear the interrupt request to the BIM. If the IRE bit in the Group BIM Control Register is set before the Compare State Register is written, another interrupt will be generated.

5.2.1.6 State On Interrupt Register

This a read only register.

Table 5-9 State On Interrupt Register

Channel Offset Read Only	7	6	5	4	3	2	1	0
$0D							SDI	SIND

The SDI and SIND bits reflect the state of the digital inputs at the moment they differ from the Compare State Register and an interrupt request is made to the Bus Interrupter Module.

5.2.1.7 Interrupt Mask Register

This register is used to specify which events should result in an interrupt asserted to the VMEbus.

Table 5-10 Interrupt Mask Register

Channel Offset Read/Write	7	6	5	4	3	2	1	0
$0F	MF_Ua2	MF_Ua1	MF_DI	MF_IND	MCAR	MBOR	MDI	MIND

MF_Ua2 When this bit is set, and the corresponding F_Ua2 bit in the Direct Input Register is set, an interrupt request to the Bus Interrupter Module (BIM) will be active.

MF_Ua1 When this bit is set, and the corresponding F_Ua1 bit in the Direct Input Register is set, an interrupt request to the Bus Interrupter Module (BIM) will be active.

MF_DI When this bit is set, and the corresponding F_DI bit in the Direct Input Register is set, an interrupt request to the Bus Interrupter Module (BIM) will be active.

MF_IND When this bit is set, and the corresponding F_IND bit in the Direct Input Register is set, an interrupt request to the Bus Interrupter Module (BIM) will be active.

MCAR When this bit is set, and the corresponding CAR bit in the Index Status Register is set, then an interrupt request to the Bus Interrupter Module (BIM) will be active.

MBOR When this bit is set, and the corresponding MOR bit in the Index Status Register is set, then an interrupt request to the Bus Interrupter Module (BIM) will be active.

MDI When this bit is set, a difference between the DI bit and the CDI bit will cause an interrupt request to the Bus Interrupter Module (BIM).

MIND When this bit is set, a difference between the IND bit and the CIND bit will cause an interrupt request to the Bus Interrupter Module (BIM).

After a SYSRESET these bits are cleared.

5.2.2 Group Fault Delay Register

This register is used to specify the delay time which must pass before a differential input is considered faulty.

Table 5-11 Group Fault Delay Register

Group Offset Read/Write	7	6	5	4	3	2	1	0
$31	D7	D6	D5	D4	D3	D2	D1	D0

Each input is continuously monitored to check whether a proper differential signal is being applied. When a non-differential signal is detected longer than the delay time, this input is considered faulty. The delay register is used to specify this delay time and can be set to a value between 0 and 255. The delay will be 100ns times the value of this register. It is recommended to use delay times longer than 500ns to prevent normal transitions of the input signals from triggering the fault detection mechanism.

5.2.3 Group Mode Register

This register is used to specify the mode a group of counters should be operated in.

Table 5-12 Group Mode Register

Group Offset Read/Write	7	6	5	4	3	2	1	0
$33						M2	M1	M0

The Group Mode Register is used to set the mode of the group’s CF32006 master device. The slave device is always in mode 0.

The following modes can be selected for the master device.

Table 5-13 CF32006 Modes

Mode	M2	M1	M0	Description
Counter Mode				
0	0	0	0	16-bit up/down counter (inhibits direction discriminator).
Direction Discriminator Mode				
1	0	0	1	Single count pulse synchronous with Ua1 rising in forward direction and Ua1 falling in backward direction.
2	0	1	0	Single count pulse synchronous with Ua2 rising in forward direction and Ua2 falling in backward direction.
3	0	1	1	Double count pulse synchronous with Ua1 rising and falling.
4	1	0	0	Double count pulse synchronous with Ua2 rising and falling.
5	1	0	1	Quadruple count pulse synchronous with all edges.
Pulse Width Measurement Mode				
6	1	1	0	Ua1 is the gate signal. Ua2 is high for up counting and low for down counting. Count is synchronous with rising 10 MHz clock.
Frequency Measurement Mode				
7	1	1	1	Ua1 is frequency signal to be measured. Ua2 is the gate signal of known time interval. Count is synchronous with rising edge of Ua1.

5.2.4 Group Reset Register

Table 5-14 Group Reset Register

Group Offset Write Only	7	6	5	4	3	2	1	0
$37								

A write access to the Group Reset Register will generate a master reset signal to the group's CF32006 device. The mode control logic is reset to a known state, and the counters are cleared.

5.2.5 Group BIM Control Register

This register is used to set different options for the BIM.

Table 5-15 Group BIM Control Register

Group Offset Read/Write	7	6	5	4	3	2	1	0
$3B	F	FAC	X/IN	IRE	IRAC	L2	L1	L0

L2, L1, L0 Interrupt level. These bits determine the level at which an interrupt will be generated. A value of zero disables the interrupt.

IRAC Interrupt Auto Clear. If the IRAC bit is set, IRE is cleared during an interrupt acknowledge cycle responding to this request. This action of clearing IRE disables the interrupt

request. To re-enable the interrupt associated with this register, IRE must be set again by writing to the Group BIM Control Register.

IRE — Interrupt Enable. This bit must be set to enable the bus interrupt request associated with this register. Thus, if the interrupt input line is asserted and IRE is cleared, no interrupt request will be asserted.

X/IN — External/Internal.
When this bit is cleared, the Interrupt Vector from the Group BIM Vector Register is presented on the data lines during an interrupt acknowledge cycle.
When this bit is '1', the BIM does not supply the vector.

Note: The X/IN must always be programmed to 0 because there is no other on-board vector source.

FAC — Flag Auto Clear. If the FAC bit is set, the Flag bit is automatically cleared during an interrupt acknowledge cycle.

F — Flag. Bit 7 is a flag that can be used in conjunction with the test and set instruction of the MC680xx. It can be changed without affecting BIM operation.

5.2.6 Group BIM Vector Register

This register contains the interrupt vector.

Table 5-16 Group BIM Vector Register

Group Offset Read/Write	7	6	5	4	3	2	1	0
$3F	V7	V6	V5	V4	V3	V2	V1	V0

This byte is presented on the data bus during an interrupt acknowledge cycle. After SYSRESET this register is set to $0F, the MC680xx un-initialized vector.

Appendix A Block Diagram

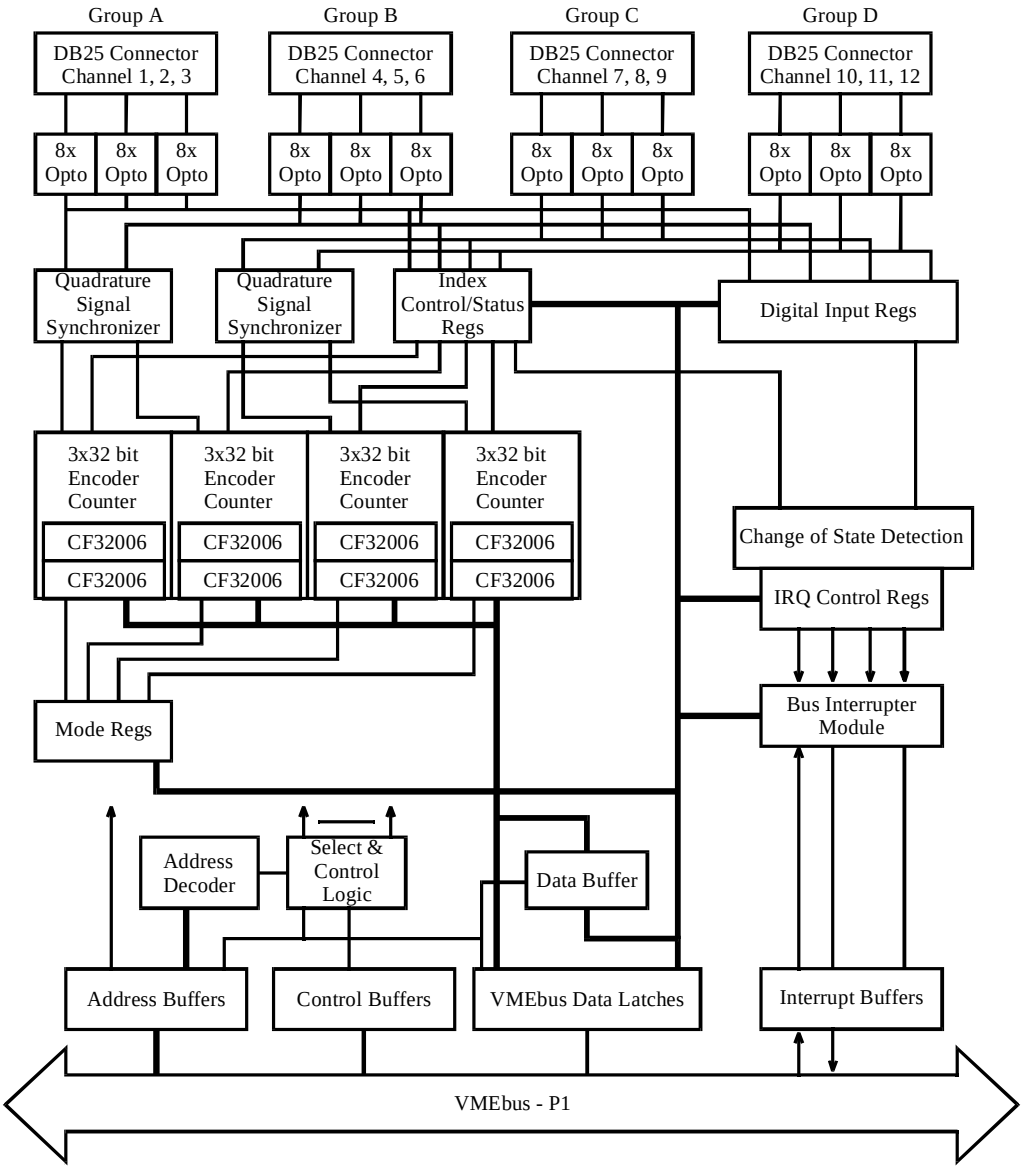


Figure A-1 Block Diagram CC433

Appendix B Schematic Diagrams

Appendix C Component Layout

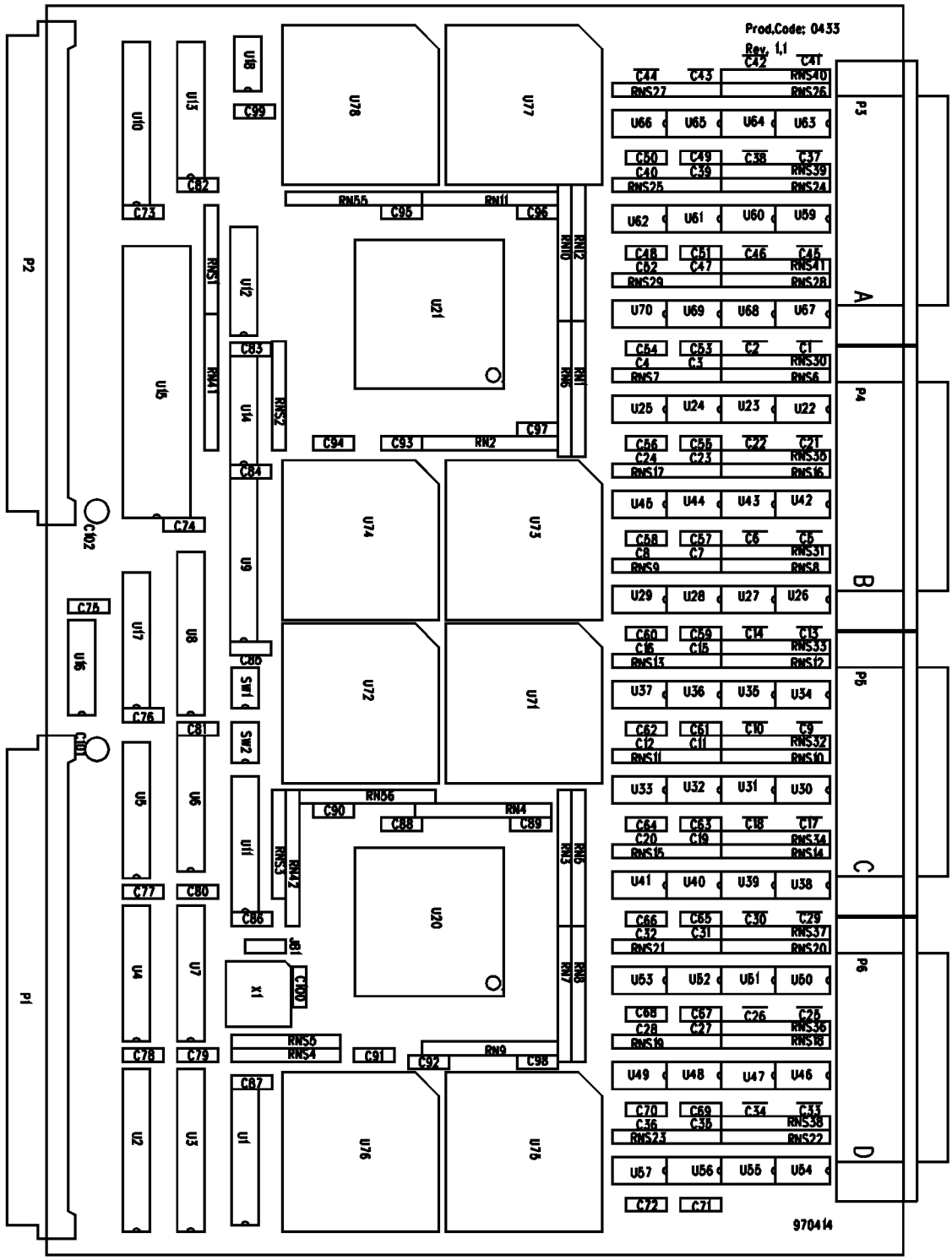


Figure C-1 Component layout CC433

Appendix D List of Components

Table D-1 List of Components

References	Component	Description
Integrated Circuits (TTL)		
U16	74F74	Dual D-type Flip-Flop
U14	74HCT157	Multiplexer
U17	74LS641-1	Hex Open Collector Buffer 48 mA
U6, U7	74LS688	8-bit Magnitude Comparator
U12	74ACT138	1-8 Decoder
U13	74HCT574	Octal D-FlipFlops
U5	74HCT573	Octal D-Latch
U1	74HCT245	Octal Bus Transceiver
U2, U3	74F543	Octal Bus Transceiver
U4	74LS240	Octal Buffers.
Integrated Circuits (PLD)		
U8	433-008-0	22V10
U9	433-009-0	22V10
U10	433-010-0	22V10
U11	433-011-0	16V8
Field Programmable Gate Array (FPGA)		
U20, U21	EPF8820AQC-4	Flex 8K FPGA
U18	EPC1231PC	Configuration prom for Flex devices
Integrated Circuits (miscellaneous)		
X1	10 Mhz	Clock oscillator
U15	68153	Bus Interrupter Module
U22-U57, U59-U70	HCPL2631	Dual Optocoupler
U71-U78	CF32006FN	Triple Incremental Encoder
Capacitors		
C1-C48	0.1 µF	Capacitor
C49-C100	0.1 µF	
C101, C102	47 µF / 10V	Capacitor, electrolytic
Resistor Networks		
RN1-RN12, RN41, RN42, RN55, RN56	4610X-101-392	3.9 kOhm pull-up 10-pin SIL
RNS1-RNS5	4608X-102-220	4x 22 Ohm Series 8-pin SIL
RNS6-RNS29	4608X-102-151	4x 150 Ohm Series 8-pin SIL
RNS30-RNS41	4608X-102-121	4x 120 Ohm Series 8-pin SIL

Table D-1 List of Components

References	Component	Description
Connectors/Jumpers		
P1-P2	96-pin	IEC-603 male
P3-P6	25 pin	D type Connector male
JB1	1x3-pin	jumper block
Switches		
SW1-SW2	DRD16C	Hex switch

Note: Some parts may have been replaced by their equivalent types.

Appendix E Connector Assignments

This Appendix identifies the VMEbus P1, VMEbus P2 and the D25 Connectors P3 to P6.

Table E-1 VMEbus P1

Pin Number	(a) Signal Mnemonic	(b) Signal Mnemonic	(c) Signal Mnemonic
1	D00	(BBSY*)	D08
2	D01	(BCLR*)	D09
3	D02	(ACFAIL*)	D10
4	D03	BG0IN*	D11
5	D04	BG0OUT*	D12
6	D05	BG1IN*	D13
7	D06	BG1OUT*	D14
8	D07	BG2IN*	D15
9	GND	BG2OUT*	GND
10	SYSCLK	BG3IN*	(SYSFAIL*)
11	GND	BG3OUT*	BERR*
12	DS1*	(BR0*)	SYSRESET*
13	DS0*	(BR1*)	LWORD*
14	WRITE*	(BR2*)	AM5
15	GND	(BR3*)	A23
16	DTACK*	AM0	A22
17	GND	AM1	A21
18	AS*	AM2	A20
19	GND	AM3	A19
20	IACK*	GND	A18
21	IACKIN*	(SERCLK)	A17
22	IACKOUT*	(SERDAT*)	A16
23	AM4	GND	A15
24	A07	IRQ7*	A14
25	A06	IRQ6*	A13
26	A05	IRQ5*	A12
27	A04	IRQ4*	A11
28	A03	IRQ3*	A10
29	A02	IRQ2*	A09
30	A01	IRQ1*	A08
31	(-12V)	(+5V STDBY)	(+12V)
32	+5V	+5V	+5V

Note: Signal mnemonics shown in parenthesis () are not used by the CC433 module.

Table E-2 VMEbus P2

P2 Pin Number	Row A Signal Mnemonic	Row B Signal Mnemonic	Row C Signal Mnemonic
1		+5 VOLT	
2		GND	
3		(RESERVED)	
4		(A24)	
5		(A25)	
6		(A26)	
7		(A27)	
8		(A28)	
9		(A29)	
10		(A30)	
11		(A31)	
12		GND	
13		+5 VOLT	
14		(D16)	
15		(D17)	
16		(D18)	
17		(D19)	
18		(D20)	
19		(D21)	
20		(D22)	
21		(D23)	
22		GND	
23		(D24)	
24		(D25)	
25		(D26)	
26		(D27)	
27		(D28)	
28		(D29)	
29		(D30)	
30		(D31)	
31		GND	
32		+5 VOLT	

Four 25-pin male “D” type connectors are available on the front panel of the module. Each connector contains signals for three input channels.

Table E-3 D25 Connectors P3 to P6

Signal Mnemonic	Pin Number	Pin Number	Signal Mnemonic
Ch1_Ua1+	1	14	Ch1_Ua1-
Ch1_Ua2+	2	15	Ch1_Ua2-
Ch1_Ind+	3	16	Ch1_Ind-
Ch1_Di+	4	17	Ch1_Di-
Ch2_Ua1+	5	18	Ch2_Ua1-
Ch2_Ua2+	6	19	Ch2_Ua2-
Ch2_Ind+	7	20	Ch2_Ind-
Ch2_Di+	8	21	Ch2_Di-
Ch3_Ua1+	9	22	Ch3_Ua1-
Ch3_Ua2+	10	23	Ch3_Ua2-
Ch3_Ind+	11	24	Ch3_Ind-
Ch3_Di+	12	25	Ch3_Di-
Not Connected	13		

Note: When inputs are single ended, connect input signals to the ’plus’ inputs (pins 1-12), and connect the ’minus’ inputs to ground (pins 14-25).

Appendix F Memory Map

Table F-1 Memory Map Group A

Name	Start	End	Size
Group A, Channel 1			
Counter	00	03	4 bytes
Enable Index Register	05	05	1 byte
Index Status Register	07	07	1 byte
Direct Input Register	09	09	1 byte
Compare State Register	0B	0B	1 byte
State on Interrupt Register	0D	0D	1 byte
Interrupt Mask Register	0F	0F	1 byte
Group A, Channel 2			
Counter	10	13	4 bytes
Enable Index Register	15	15	1 byte
Index Status Register	17	17	1 byte
Direct Input Register	19	19	1 byte
Compare State Register	1B	1B	1 byte
State on Interrupt Register	1D	1D	1 byte
Interrupt Mask Register	1F	1F	1 byte
Group A, Channel 3			
Counter	20	23	4 bytes
Enable Index Register	25	25	1 byte
Index Status Register	27	27	1 byte
Direct Input Register	29	29	1 byte
Compare State Register	2B	2B	1 byte
State on Interrupt Register	2D	2D	1 byte
Interrupt Mask Register	2F	2F	1 byte
Group A			
Fault Detect Delay Register	31	31	1 byte
Mode Register	33	33	1 byte
Reset Register	37	37	1 byte
BIM Control Register	3B	3B	1 byte
BIM Vector Register	3F	3F	1 byte

Table F-2 Memory Map Group B

Name	Start	End	Size
Group B, Channel 4			
Counter	40	43	4 bytes
Enable Index Register	45	45	1 byte
Index Status Register	47	47	1 byte
Direct Input Register	49	49	1 byte
Compare State Register	4B	4B	1 byte
State on Interrupt Register	4D	4D	1 byte
Interrupt Mask Register	4F	4F	1 byte
Group B, Channel 5			
Counter	50	53	4 bytes
Enable Index Register	55	55	1 byte
Index Status Register	57	57	1 byte
Direct Input Register	59	59	1 byte
Compare State Register	5B	5B	1 byte
State on Interrupt Register	5D	5D	1 byte
Interrupt Mask Register	5F	5F	1 byte
Group B, Channel 6			
Counter	60	63	4 bytes
Enable Index Register	65	65	1 byte
Index Status Register	67	67	1 byte
Direct Input Register	69	69	1 byte
Compare State Register	6B	6B	1 byte
State on Interrupt Register	6D	6D	1 byte
Interrupt Mask Register	6F	6F	1 byte
Group B			
Fault Detect Delay Register	71	71	1 byte
Mode Register	73	73	1 byte
Reset Register	77	77	1 byte
BIM Control Register	7B	7B	1 byte
BIM Vector Register	7F	7F	1 byte

Table F-3 Memory Map Group C

Name	Start	End	Size
Group C, Channel 7			
Counter	80	83	4 bytes
Enable Index Register	85	85	1 byte
Index Status Register	87	87	1 byte
Direct Input Register	89	89	1 byte
Compare State Register	8B	8B	1 byte
State on Interrupt Register	8D	8D	1 byte
Interrupt Mask Register	8F	8F	1 byte
Group C, Channel 8			
Counter	90	93	4 bytes
Enable Index Register	95	95	1 byte
Index Status Register	97	97	1 byte
Direct Input Register	99	99	1 byte
Compare State Register	9B	9B	1 byte
State on Interrupt Register	9D	9D	1 byte
Interrupt Mask Register	9F	9F	1 byte
Group C, Channel 9			
Counter	A0	A3	4 bytes
Enable Index Register	A5	A5	1 byte
Index Status Register	A7	A7	1 byte
Direct Input Register	A9	A9	1 byte
Compare State Register	AB	AB	1 byte
State on Interrupt Register	AD	AD	1 byte
Interrupt Mask Register	AF	AF	1 byte
Group C			
Fault Detect Delay Register	B1	B1	1 byte
Mode Register	B3	B3	1 byte
Reset Register	B7	B7	1 byte
BIM Control Register	BB	BB	1 byte
BIM Vector Register	BF	BF	1 byte

Table F-4 Memory Map Group D

Name	Start	End	Size
Group D, Channel 10			
Counter	C0	C3	4 bytes
Enable Index Register	C5	C5	1 byte
Index Status Register	C7	C7	1 byte
Direct Input Register	C9	C9	1 byte
Compare State Register	CB	CB	1 byte
State on Interrupt Register	CD	CD	1 byte
Interrupt Mask Register	CF	CF	1 byte
Group D, Channel 11			
Counter	D0	D3	4 bytes
Enable Index Register	D5	D5	1 byte
Index Status Register	D7	D7	1 byte
Direct Input Register	D9	D9	1 byte
Compare State Register	DB	DB	1 byte
State on Interrupt Register	DD	DD	1 byte
Interrupt Mask Register	DF	DF	1 byte
Group D, Channel 12			
Counter	E0	E3	4 bytes
Enable Index Register	E5	E5	1 byte
Index Status Register	E7	E7	1 byte
Direct Input Register	E9	E9	1 byte
Compare State Register	EB	EB	1 byte
State on Interrupt Register	ED	ED	1 byte
Interrupt Mask Register	EF	EF	1 byte
Group D			
Fault Detect Delay Register	F1	F1	1 byte
Mode Register	F3	F3	1 byte
Reset Register	F7	F7	1 byte
BIM Control Register	FB	FB	1 byte
BIM Vector Register	FF	FF	1 byte