Technical Manual CC92
Isolated Digital Input Board
Version 1.3 March 1991

Chapter 1

General Information

1.1 Introduction

This manual provides information for use, installation instructions and theory of operation for the CC92 VMEbus isolated digital input board.

1.2 Features of the Module

- Double Eurocard form factor
- full interrupt capability
- 32 isolated digital inputs grouped in 4 independent channels
- occupies 32 memory locations in short I/O space
- board can be made accessible in supervisory mode only or
- in both supervisory and non-privileged mode
- each channel has:
- 8 optically coupled input networks with reverse bias, over-voltage protection, and debouncing
- a change of state circuit for standard CC92 modules
- a pattern check circuit for CC92 B type modules
- its own interrupt level
- its own interrupt vector
- its own interrupt mask

1.3 General Description

The CC92 isolated digital input board is a VME slave module. The module only decodes address lines A1 to A15 and only responds when receiving the address modifier codes $29 and/or $2D (short supervisory/non-privileged I/O access).

The module appears to the system as 32 byte locations which can be placed on every 32 byte boundary in the 64 kByte short address space.

The module consists of 4 fully independent channels with 8 inputs each. Each channel is capable to detect a change in any of its input lines and may generate an interrupt when it detects such a change. For the B type modules, the change of state circuit is replaced with a circuit that compares the input pattern with a defined pattern and may generate an interrupt when a match is detected. The used interrupter module is a MC68153 (BIM) which has a software programmable interrupt level, interrupt vector and interrupt mask for each of the four channels.

1.4 Specifications

1.4.1 VMEbus

Slave data transfer options:

- A16:D8

Interrupt options:

- any one of I(1), I(2), I(3), I(4), I(5), I(6), I(7) DYN

Power requirements:

- 1.00 Amp typical. at +5Vdc

Physical configuration:

- NEXP

1.4.2 Electrical

Table 1-1 Electrical characteristics

	24 Volt	TTL
Voltage sense:		
logic 0	4Vdc	2Vdc
logic 1	17Vdc	3.5Vdc
Input characteristics		
number of inputs	32	32
input resistor	10k 1/2W	1k 1/2W
Maximum voltage across input without damage		
	70 Vdc	20 Vdc
	140 Vac, rms	40 Vac, rms

Delay times:

- open-to-closed: 10 msec.
- closed-to-open: 10 msec.

Isolation voltage:

- system-to-field: 500 Vdc
- channel-to-channel: 300 Vdc

Environmental conditions:

- operational temperature: 0 - 70 degrees C
- maximum operating humidity: 90%

1.4.3 Mechanical

Two 37-pin male "D" type connectors on board for input connections.

Use AMP type 206655-1 (or equivalent) as mating connector.

Chapter 2

Installation Instructions

2.1 Introduction

This chapter provides the preparation and installation instructions for the CC92 isolated digital input board.

2.2 Installation

The module can be used in VMEbus systems. Before use the jumpers and switches must be checked.

2.3 Cable Connections

The 32 I/O lines are available through the two connectors P3 and P4 on the front panel.

The following table shows the connector pin lay-out.

Table 2-1 P3 and P4 connector layout

Pin		P3	P4
(+)	(-)		
1	20	input 0	input 16
2	21	input 1	input 17
3	22	input 2	input 18
4	23	input 3	input 19
5	24	input 4	input 20
6	24	input 5	input 21
7	26	input 6	input 22
8	27	input 7	input 23
9	28	input 8	input 24
10	29	input 9	input 25
11	30	input 10	input 26
12	31	input 11	input 27
13	32	input 12	input 28
14	33	input 13	input 29
15	34	input 14	input 30
16	35	input 15	input 31
17	36	NC	NC

Table 2-1 P3 and P4 connector layout

Pin		P3	P4
18		NC	NC
19	37	NC	NC

2.4 Jumper Settings

The jumper settings discussed in the next section are illustrated as seen from the component side with the VMEbus connector downwards.

2.4.1 Base address selection

The CC92 module occupies 32 memory locations in the 64k short I/O memory space. With the hex switches S1, S2 and S3 the base address can be set on a 32 byte boundary. S3 selects the address lines A5 to A7, S2 the address lines A8 to A11 and S1 the address lines A12 to A15.

2.4.2 Address modifier

The module responds to 1 or 2 address modifier codes. JB1 selects whether the module can be accessed in supervisory mode only or in both supervisory and non-privileged mode.

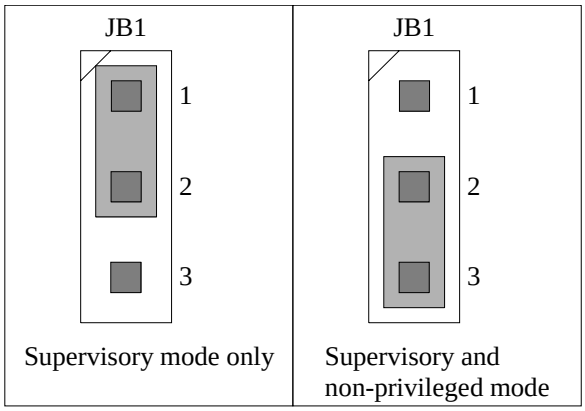

Figure 2-1 Address Modifier Jumper

In supervisory mode the CC92 module only responds to AM code $2D while in supervisory and non-privileged mode it responds to AM codes $29 and $2D.

Chapter 3

Programming Considerations

3.1 Introduction

This section contains information for system programmers to take full advantage of the features of the CC92 module.

3.2 Memory Map Layout

Table 3-1 Address select

A4	A3	register select
0	0	BIM control register
0	1	BIM vector register
1	0	Current/Compare State register
1	1	Change State Register

A2	A1	channel select
0	0	channel 0
0	1	channel 1
1	0	channel 2
1	1	channel 0

The next table shows all registers with their respective offsets to the module's base address.

Table 3-2 Memory Map Layout

Offset	Contents
01	Control Register Channel 0 Level/interrupt bits
03	Control Register Channel 1 Level/interrupt bits
05	Control Register Channel 2 Level/interrupt bits

Table 3-2 Memory Map Layout

Offset	Contents
07	Control Register Channel 3 Level/interrupt bits
09	Vector Register Channel 0
0B	Vector Register Channel 1
0D	Vector Register Channel 2
0F	Vector Register Channel 3
11	Read Current State Register Channel 0 Write Compare State Register
13	Read Current State Register Channel 1 Write Compare State Register
15	Read Current State Register Channel 2 Write Compare State Register
17	Read Current State Register Channel 3 Write Compare State Register
19	Read Change State Register Channel 0
1B	Read Change State Register Channel 1
1D	Read Change State Register Channel 2
1F	Read Change State Register Channel 3

3.3 The 68153 Bus Interrupter Module

The MC68153 Bus Interrupter Module (BIM) is designed to serve as an interrupt requester for peripheral devices in a microcomputer system. Up to four independent devices can be interfaced to the system bus by the MC68153. Intended for asynchronous master/slave bus operation, the BIM is compatible with VMEbus. An interrupt request from any device is routed to the MC68153, and the BIM handles all interface to the system bus. It generates a bus interrupt request as a result of the device interrupt request. When the system interrupt handler responds with an interrupt acknowledge cycle, the MC68153 can answer supplying an interrupt vector and handling all timing.

Four 8-bit vector registers contain status/address information and supply a byte vector in response to an interrupt acknowledge cycle for the corresponding interrupt source. Four other 8 bit control registers contain information that oversees operation of the interrupt circuitry. The control information is programmable and includes interrupt request level and interrupt enable and disable. Also contained in the control register are flag bits. These flags are useful for task coordination, resource management, and interprocessor communication.

3.4 The channel registers

Each of the four channels occupies 4 addresses.

Table 3-3 Channel Registers

channel offset	Read	Write
1	BIM Control	BIM Control
9	BIM Vector	BIM Vector
11	Current State	Compare State
19	Change State	-

The first address is the control register supplied by the BIM. It is used to set the interrupt level and the interrupt enable bits of a channel.

The second address is the vector register supplied by the BIM. The Current State Register supplies the current state of the input signals. An input voltage lower than 4 Vdc on the input port is read as a ’0’. An input voltage higher than 17 Vdc on the input port is read as a ’1’.

The Current State Register is a read only register. The following table shows the Current State Register bit assignment for the four channels.

Table 3-4 Current State Register Bit

Channel	Bit	Input
0	0 .. 7	0 .. 7
1	0 .. 7	8 .. 15
2	0 .. 7	16 .. 23
3	0 .. 7	24 .. 31

The Compare State Register is used by the Change of State Circuit. The contents of this register is continuously compared with the state of the inputs. When a mismatch is detected an interrupt request is generated to the BIM. The Compare State Register is a write only register.

The contents of the Change State Register is set by the Change of State Circuit. It holds the 8-bit image of the state of the inputs which caused the Change of State interrupt. The Change State Register is a read only register.

3.5 Using the Change of State Circuitry

If it is desired to detect changes in the input lines without continuously polling the inputs, the Change of State circuit must be used.

To activate this circuit certain actions are to be performed by the user, in a certain sequence.

There are four channels and they may, independently from each other, be configured to generate interrupts. All actions which are now to be described are related to one of the four channels.

First the contents of the Compare State Register must be initialized with the desired compare pattern. Note: Normally this will be the current state of the inputs read from the Current State Register. Next the contents of the interrupt vector register must be initialized with the desired vector information. Last the contents of the control register of the BIM must be initialized with the desired interrupt level and with the interrupt enable bit SET and the interrupt auto-clear bit SET and the Ex/Int bit RESET.

When a change in the input lines is detected an interrupt is generated on the desired level and an acknowledge will be answered with the desired vector. The interrupt auto-clear bit must be set to automatically remove the interrupt from the bus when it is acknowledged.

The Change of State circuit samples the current state of the input lines into the Change State Register when the first difference is detected between the input lines and the contents of the Compare State Register. The Change State Register may be read after an interrupt has occurred to determine what change did generate the interrupt. Reading this register does not alter its contents, however reading the Current State Register DOES change the contents of the Change State Register. Thus, when an interrupt has occurred first the Change State Register should be examined. Also, no read of the Current State Register should occur while waiting for an interrupt because reading the Current State Register may invalidate the contents of the Change State Register.

3.6 Using the Pattern Check Circuitry

This section applies to the CC92 B type modules. For the CC92 B type modules, the change of state circuit is replaced with the pattern check circuitry.

The difference between the Pattern Check and the Change of State circuit is that the pattern check circuit can generate an interrupt when a defined pattern is detected at the inputs, and the Change of State circuit can generate an interrupt when an input change is detected.

For detailed description refer to section 3.5 “Using the Change of State Circuitry”.

3.7 Reset

The reset signal from the VMEbus will reset the BIM control registers to all zero's (the interrupt enable bits are cleared) and the vector registers to the value $0F. This is the uninitialized vector for the MC68000. No other registers on the board are affected by a reset.

Chapter 4

Theory of Operation

4.1 Introduction

This chapter provides a description of the CC-92 isolated digital input module. The block diagram is given in Appendix A.

4.2 Address Selection

Address lines A15 to A5 and address modifier lines AM5 to AM0 are compared (by U60 and U66) with the setting of the switches S1 to S3, and the jumper block JB1. When a match is found and the address strobe is active the board select signal (/bs) is generated. The pal U61 decides, depending on the value of A4, if either the BIM or one of the channel registers is selected. The channel register select signals are distributed to one of the four channels by U47 and U54, depending on the values of A2 and A3. The board responds on odd and even byte addresses but only on odd addresses relevant data is transferred.

4.3 Dtack Generation

Dtack is generated whenever the board is selected or when an interrupt acknowledge cycle is performed. The Dtack timer is started immediately when a channel register is selected (A4 is high). When the BIM is selected (A4 is low) the Dtack timer is started when the BIM asserts its DTACK output.

During an interrupt acknowledge cycle the Dtack timer is started when the BIM asserts its INTAE output. The Dtack timer is started by deasserting the CLRDT signal to the shift register U53. The clock input of this register is connected to the 16 Mc clock and will shift a '1' into the register. After four clock periods output 4D will go high and DTACK* is asserted on the bus.

4.4 Input Circuitry

The board is divided into four channels, each consisting of eight inputs. Each individual input consist of:

- a current limiting resistor (R4-R35),
- a bias resistor (R36-R67),
- a reverse current protection diode (D1-D32),
- an opto-coupler IC (U1-U32),
- a pull-up resistor (RN4-RN7) and
- a debounce circuit (U34, U36, U38, U40, U43 and U45).

The current limiting and the bias resistors determine the “on” and “off” input current values.

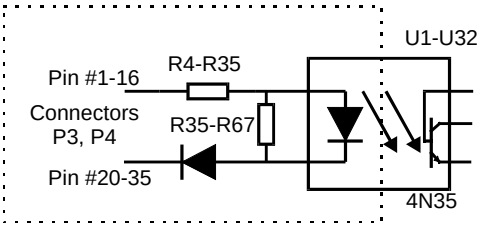

Figure 4-1 Input Network

The debounce circuit has a programmable debounce time which is set by the value of C2 following the equation:

$$T = 2,13 \times C_2, \text{ where}$$
$$C_2 = \text{picofarads; and}$$
$$T = \mu\text{seconds}$$

The debounce IC U40 is used to generate the debounce clock. This clock is fed to the other debounce IC's U34, U36, U38, U43 and U45 through U47. U47 is used as a non-inverting buffer. Data from the debouncers have an inverted polarity.

4.5 Data Circuit

The current state of the inputs of a channel can be read through an 8 bit edge clocked inverting buffer (U41, U42, U44 and U46). When the buffer is addressed, the clock input will go high, sampling the current state of the outputs of the debounce circuits of the channel. Also the outputs of the buffer will be enabled. As long as the read operation continues, changes in the debounce outputs will have no effect on the data read.

4.6 Change of State Circuit

This circuit is designed to generate an interrupt whenever the inputs of a channel do not match with an user defined pattern.

To accomplish this the following blocks are defined:

1. the input signals read from the debounce circuit outputs (U34, U36, U38, U40 and U43)
2. an 8 bit register (U33, U35, U37 and U39), which contents is defined by the user, identified as the Compare State Register
3. an 8 bit pattern comparator (U48, U49, U51 and U52) which detects differences between the outputs of the debouncer and the outputs of the Compare State Register
4. memory element (U50) to remember that a difference between the state of the input lines and the pattern of the Compare State Register has existed.

5. a sample pulse generator (U50 and U58)
6. a register to hold the state of the inputs when the difference was detected, identified as the Change State Register (U41, U42, U44 and U46)

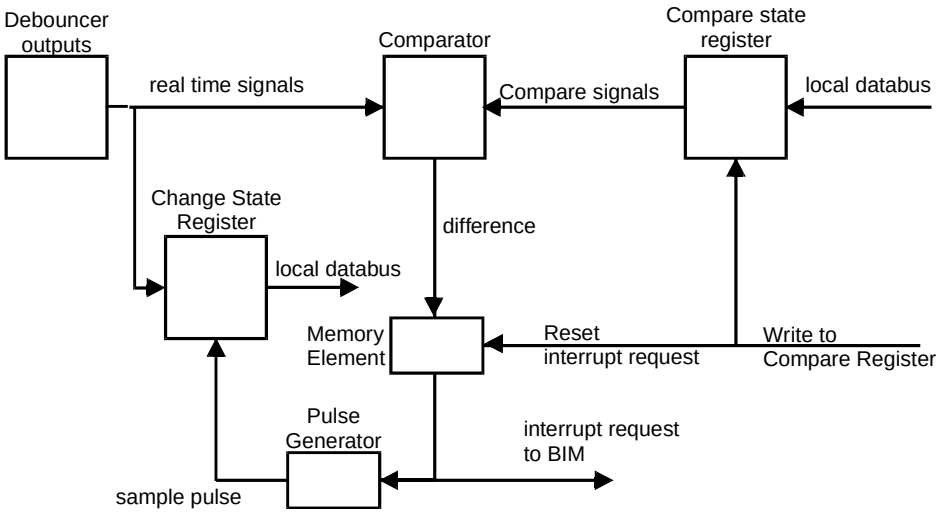

Figure 4-2 Change of State Circuit

To detect a change in the input lines the pattern comparator must compare the “Real Time” input lines with a copy of the old state of the input lines. Thus a copy should be made of the present state of the input lines, by reading the Current State Register, and this data should be written into the Compare State Register.

Writing to this Compare State Register resets the memory element to a “no-interrupt” status. The output of the comparator should now be inactive (no differences). The output of the comparator will go active (a difference) as soon as one or more of the inputs change their level. The memory element is set to the “interrupt” status and asserts the interrupt request line to the BIM. Also the sample pulse generator is triggered and a sample of the outputs of the debouncer is stored in the Change State Register. Data read from this Change State Register will now reflect the state of the input lines when the change was detected.

4.7 Pattern Check Circuit

As described in chapter three, the change of state circuit is replaced with a pattern check circuit for the B type CC92 modules.

The theory of operation for this circuit is the same as described in the previous section for the change of state circuit, except that the B type modules can generate an interrupt when the input patter matches the defined pattern written into the compare state register.

Appendix A Block Diagram

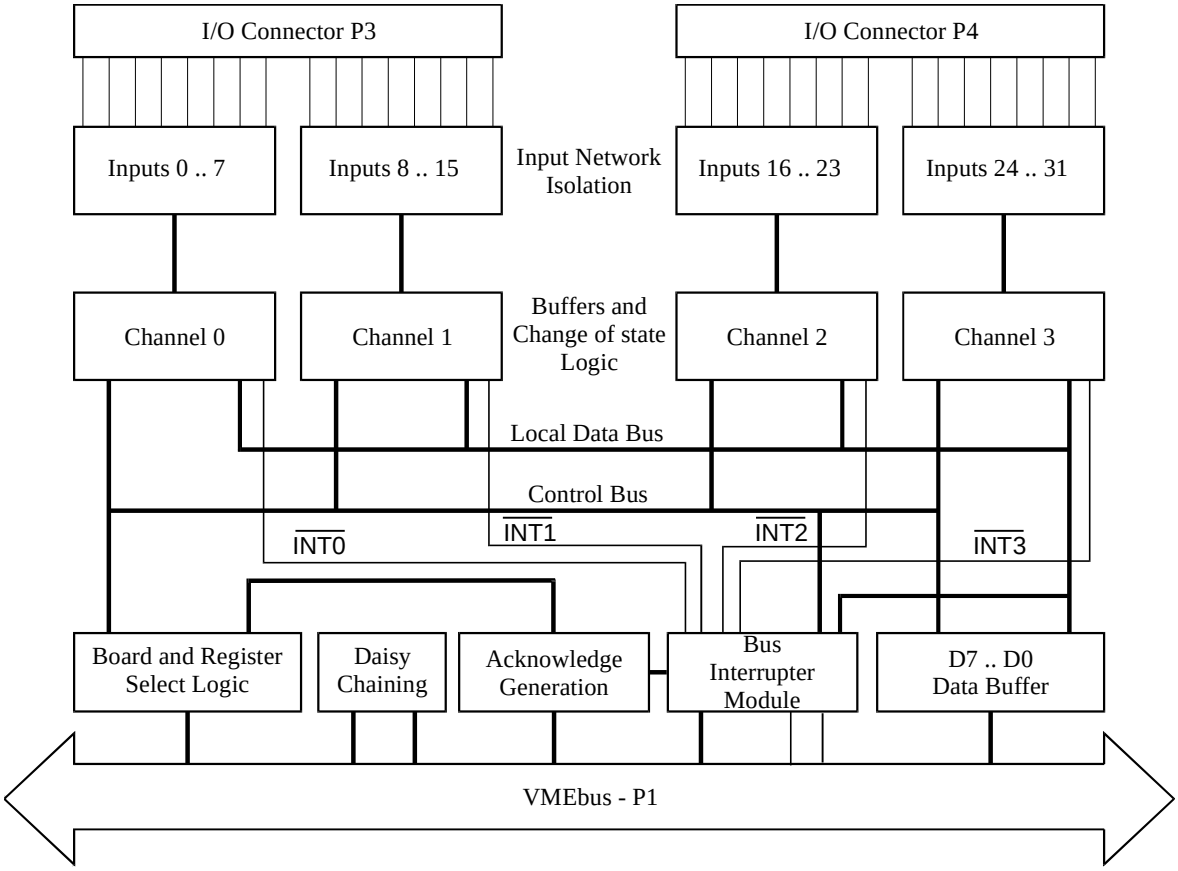

Figure A-1 CC92 Block Diagram

Appendix B Photo CC92 Board

Placeholder

Figure B-1 Photo CC92 Board