Technical Manual CC94
Isolated Output Board
Version 1.1 December 1989

Chapter 1

General Information

1.1 Introduction

This manual provides information for use, installation instructions and theory of operation for the CC94 VMEbus isolated output board.

1.2 Features of the Module

- Double Eurocard form factor
- 32 isolated digital outputs grouped in 4 independent channels
- each channel has 8 isolated output networks with contact transient protection
- occupies 8 memory locations in short I/O space
- board can be made accessible in supervisory mode only or in both supervisory and non-privileged mode

1.3 General Description

The CC94 isolated output board is a VME slave module. The module decodes address lines A1 to A15 and only responds when receiving the address modifier codes $29 and/or $2d (short supervisory/non-privileged I/O access).

The module appears to the system as 8 byte locations which can be placed on every 8 byte boundary in the 64 kByte short address space.

Each channel appears to the system as an 8 bit memory location.

Data written to the outputs is latched and can be read back. On board “Power On” reset circuit de-activates all outputs. Outputs are optionally de-activated by SYSRES*.

1.4 Ordering Information

Table 1-1 Ordering Information

module	contact	load	de-activated state
CC94NO	reed relays	AC	open
CC94NC	reed relays	AC	closed
CC94SS	solid state	DC	open

1.5 Specifications

1.5.1 VMEbus

Slave data transfer options:

- A16:D8(EO)

Power requirements:

- 0.6 A at +5Vdc (1.0 A max.)

Physical configuration:

- NEXP

1.5.2 Electrical

Digital output

Table 1-2 Digital Output Specifications

Type (resistive loads)	CC94NO	CC94NC	CC94SS	Unit
Watts DC max.	10	10	5	W
Amps max.	0.500	0.500	0.250	A
Voltage max.	28	28		Vrms
Voltage max.			28	Vdc
Life min.	5x10e6	5x10e6	>5x10e6	operations
Init. contact res. max.	0.2	0.2		Ohm
Output voltage drop max.			0.6	Vdc
Actuate time max.	250	200	1	µSec
De-Actuate time max. (bounce included)	200	350	5	µSec

Transient protection

- Continuous power rating: 250 mW
- Discharge capacity: 30 watt-seconds
- Leakage current through transient suppressor at 28 V: 5 mA

Isolation voltage:

- system-to-field: 500 Vdc
- channel-to-channel: 300 Vdc

Environmental conditions:

- operational temperature: 0 - 70 degrees C
- maximum operating humidity: 90%

1.5.3 Mechanical

Two 37-pin female “D” type connectors on board for output connections.

Chapter 2

Installation Instructions

2.1 Introduction

This chapter provides the preparation and installation instructions for the CC94 isolated output board.

2.2 Installation

The module can be used in VMEbus systems. Before use the jumpers and switches must be checked.

2.3 Cable Connections

The 32 I/O lines are available through the two connectors P3 and P4 on the front panel. The following table shows the connector pin layout.

Table 2-1 P3, P4 Pin Layout

(+)	(-)	P3	P4
1	20	output 0	output 16
2	21	output 1	output 17
3	22	output 2	output 18
4	23	output 3	output 19
5	24	output 4	output 20
6	25	output 5	output 21
7	26	output 6	output 22
8	27	output 7	output 23
9	28	output 8	output 24
10	29	output 9	output 25
11	30	output 10	output 26
12	31	output 11	output 27
13	32	output 12	output 28
14	33	output 13	output 29
15	34	output 14	output 30
16	35	output 15	output 31
17	36	+5V	+5V
18		NC	NC
19	37	COMMON	COMMON

2.4 Jumper Settings

The jumper settings discussed in the next section are illustrated as seen from the component side with the VMEbus connector downwards.

2.4.1 Base Address Selection

The CC94 module occupies 8 memory locations in the 64k short I/O memory space. With the hex switches S1, S2 and S3 and jumper block JB1 the base address can be set on an 8 byte boundary. JB1 selects address line A3.

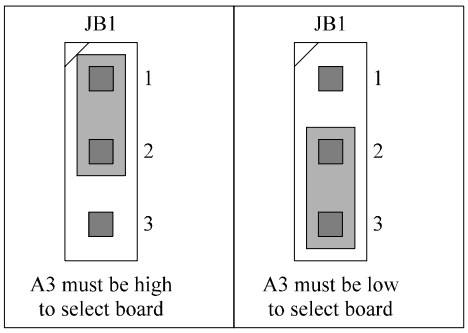

Figure 2-1 JB1: Base Address Selection

S3 selects the address lines A4 to A7, S2 the address lines A8 to A11 and S1 the address lines A12 to A15.

2.4.2 Address Modifier

The module responds to 1 or 2 address modifier codes. JB2 selects whether the module can be deceased in supervisory mode only or in both supervisory and non-privileged mode.

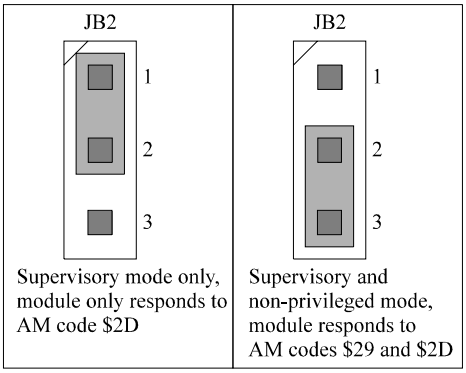

Figure 2-2 JB2: Address Modifier

2.4.3 Reset Option

JB3 selects whether a SYSRES* affects the state of the outputs or not.

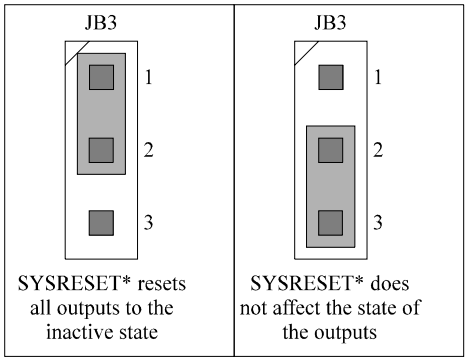

Figure 2-3 JB3: SYSRESET*

Chapter 3

Programming Considerations

3.1 Introduction

This section contains information for system programmers to take full advantage of the features of the CC94 module.

3.2 Memory Map Layout

The following table shows the registers with their respective offsets to the module's base address.

Table 3-1 Register Offsets

Offset	Contents
01	Read/Write Output Register Channel 0
03	Read/Write Output Register Channel 1
05	Read/Write Output Register Channel 2
07	Read/Write Output Register Channel 3

An output is activated when the corresponding bit in the output register is set (1). An output is de-activated when the corresponding bit in the output register is reset (0). The state of 8 outputs are defined by a single 8 bit write operation to the proper channel. The state of a single output can be changed with a bit_set or bit_clear operation on the proper output bit. The following table shows the Output Register bit assignment for the four channels.

Table 3-2 Output Register Assignments

Channel	Bit	Output
0	0 .. 7	0 .. 7
1	0 .. 7	8 .. 15
2	0 .. 7	16 .. 23
3	0 .. 7	24 .. 31

3.3 Reset

At power on an on board circuit ensures that all outputs become in a de-activated state.

Jumper JB3 is provided to allow SYSRES* to affect the state of the outputs. When JB3 is not installed, a SYSRES* does not alter the state of the outputs. When JB3 is installed, a SYSRES* will reset all outputs to the de-activated state.

Chapter 4

Theory of Operation

4.1 Introduction

This chapter provides a description of the CC94 isolated output module. The block diagram is given in Appendix A

4.2 Address Selection

Address lines A15 to A3 and address modifier lines AM5 to AM0 are compared (by U47 and U48) with the setting of the switches S1 to S3, and the jumperblocks JB1 and JB2. When a match is found and the address strobe is active the board select signal (/bs) is generated. The “read register” and “write register” signals are distributed to one of the four channels by U49, depending on the values of A1 and A2. The board responds on odd and even byte addresses but only on odd addresses relevant data is transferred.

4.3 Dtack Generation

Dtack is generated whenever the board is selected. The Dtack timer is started by deasserting the “clrdt” signal to the shift register U51. The clock input of this register is connected to the 16 Mc clock and will shift a '1' into the register. After four clock periods output U51-pin6 will go high and DTACK* is asserted on the bus.

4.4 Output Circuitry

The board is divided into four channels, each consisting of eight outputs. Each individual output consist of:

- a D-type register with read-back (U41-U44, U37-U40)
- a high-current output driver (U33-U36)
- a relay with a fly-back diode (U1-U32, D1-D32) and
- a metal oxide varistor transient suppressor (V1-V32).

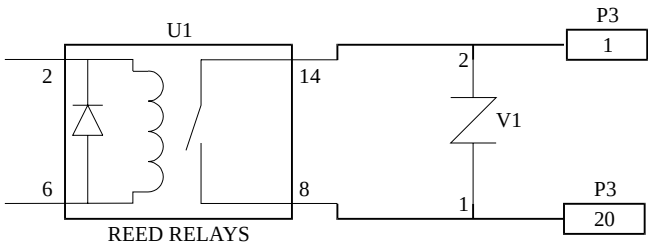

Figure 4-1 Output Network

4.5 Reset Circuitry

At power on the 555 timer (U55) holds “lreset” active for 100 ms. During this time, SYSFAIL* is asserted on the VMEbus.

When JB3 is installed, a SYSRES* from the VMEbus also makes “lreset” active.

Appendix A Block Diagram

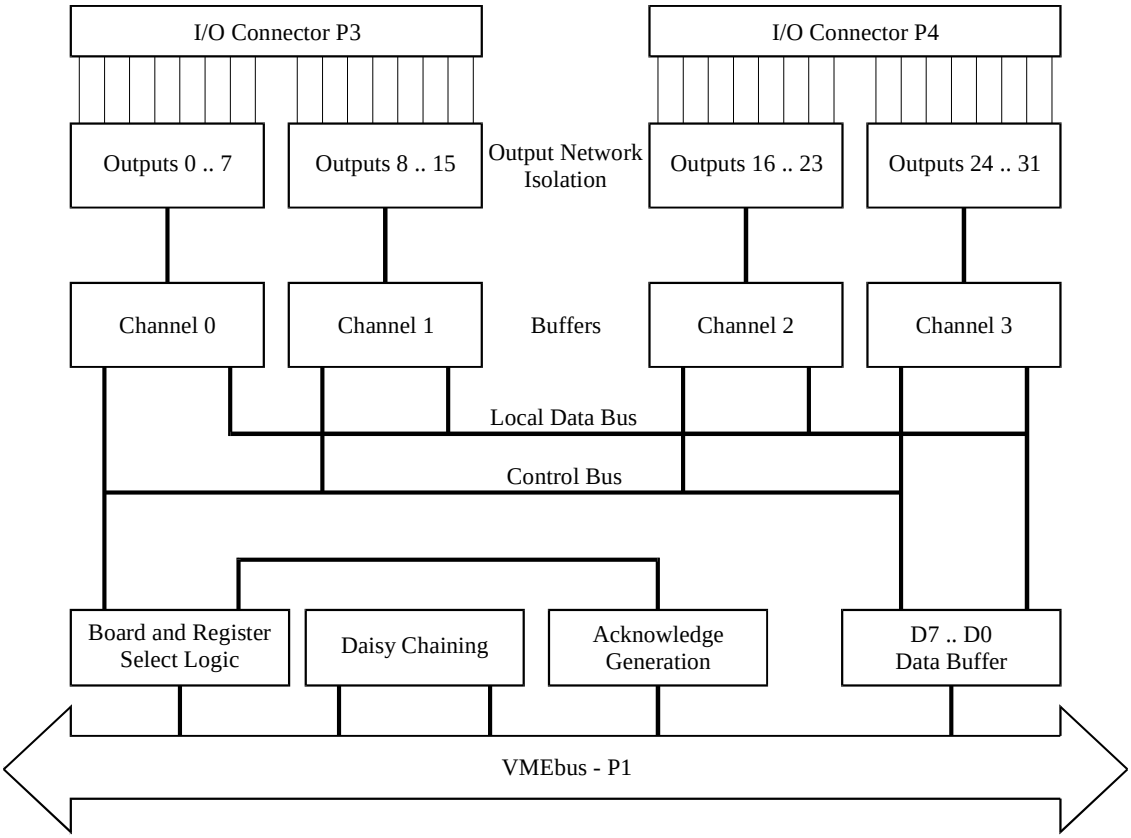

Figure A-1 Block Diagram

Appendix B Photo CC94 Board

Placeholder

Figure B-1 Photo CC94 Board